

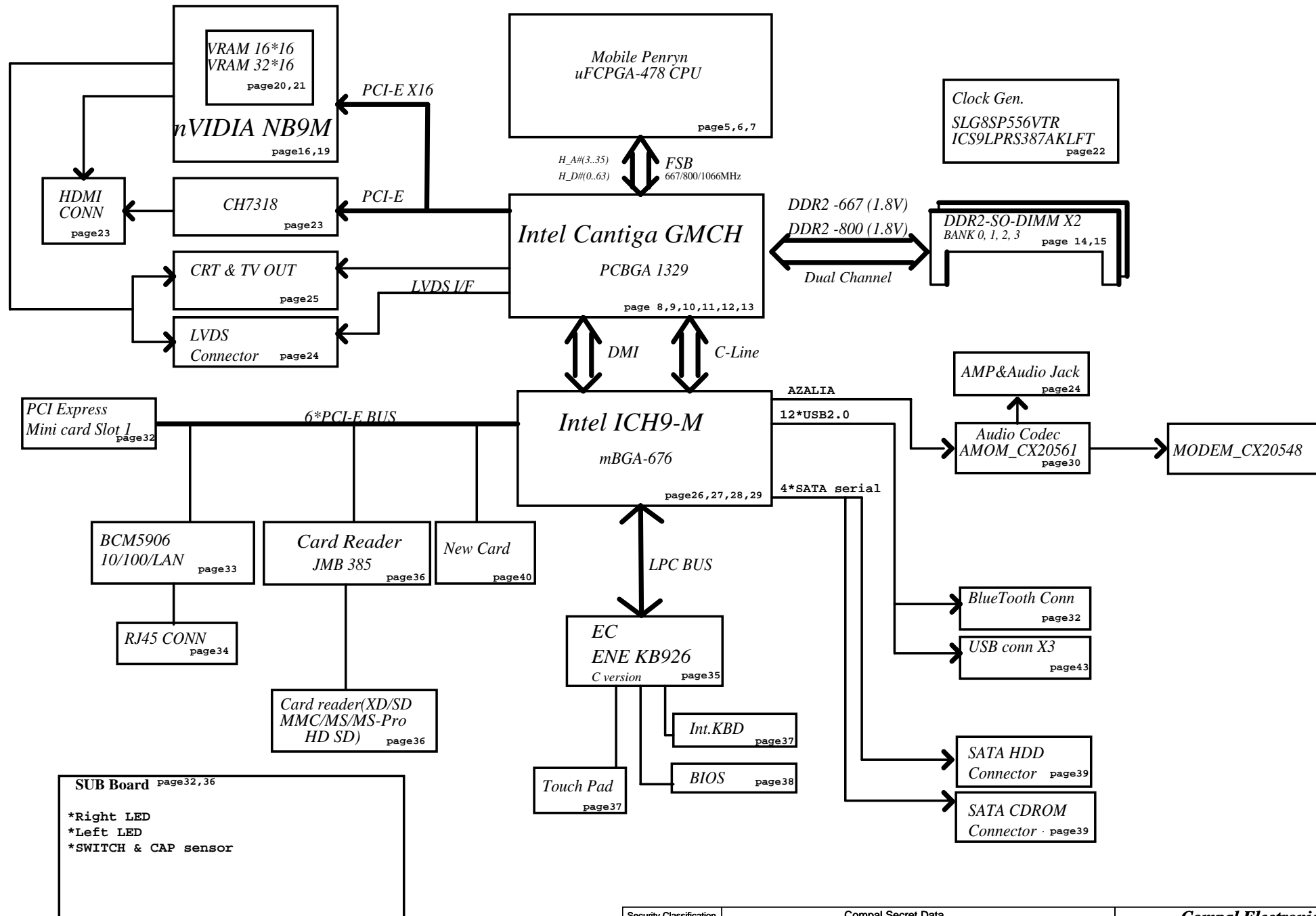
JIWA1/A2

Compal ~~confidential~~ Schematic Document
Mobile Penryn uFCPGA
Intel Cantiga_GM/PM+ICH9-M

Saturday, June 06, 2009

REV:2.0

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM@
GM@
X76@

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+1.1VS	1.1V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

EDP at Tj = 97C*

Power Supply Rail		NB9M-GS		NB9M-GE	
	(V)	GDDR3	DDR2	GDDR3	DDR2
NVVD	Variable	12.68A	11.57A	10.52A	9.59A
FB_DLLAVDD	1.1	25mA			
FB_PLLAVDD	1.1	10mA			
IFPC_IOVDD	1.1	385mA			
IFPD_IOVDD	1.1	385mA			
IFPE_IOVDD	1.1	385mA			
IFPF_IOVDD	1.1	385mA			
PEX_IOVDD/Q	1.1	1400mA			
PEX_PLLVDD	1.1	110mA			
PLLVD	1.1	65mA			
SP_PLLVDD	1.1	25mA			
VID_PLLVDD	1.1	50mA			
TOTAL	1.1	3.225A			
FBVDD/Q	1.8	3080mA	1720mA	3010mA	1680mA
IFPA_IOVDD	1.8	50mA			
IFPB_IOVDD	1.8	50mA			
IFPAB_PLLVDD	1.8	100mA			
IFPCD_PLLVDD	1.8	160mA			
IFPEF_PLLVDD	1.8	160mA			
TOTAL	1.8	3.6A	2.24A	3.53A	2.2A
DACA_VDD	3.3	130mA			
DACB_VDD	3.3	255mA			
DACC_VDD	3.3	130mA			
MIOA_VDDQ	3.3	10mA			
MIOB_VDDQ	3.3	10mA			
VDD33	3.3	110mA			
TOTAL	3.3	0.645A			

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

POWER SEQUENCE

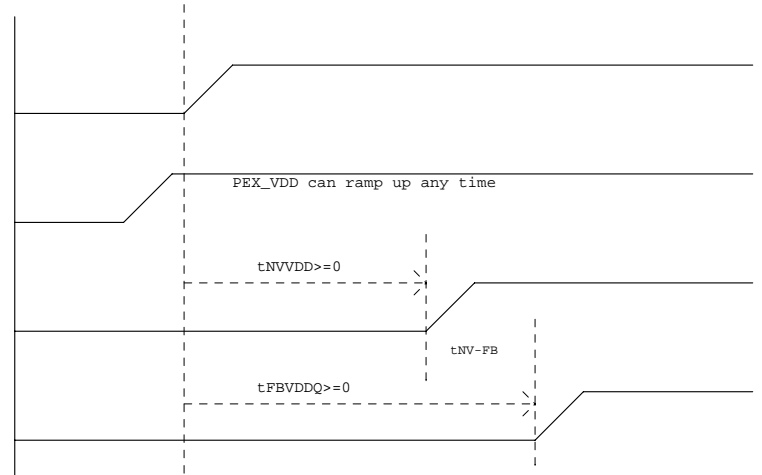
The ramp time for any rail must be more than 40us

(+3VS) VDD33

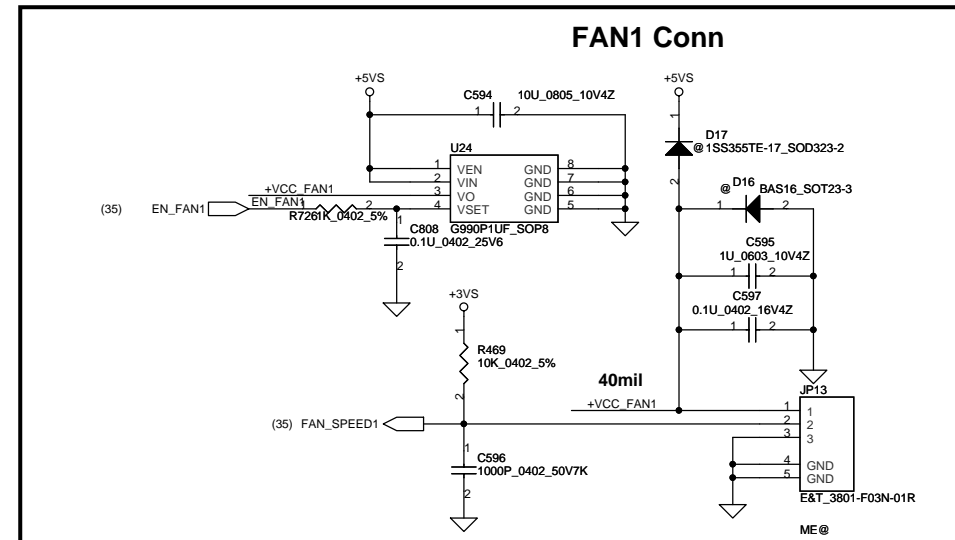
(1.1VS) PEX_VDD

(+VGA_CORE) NVVD

(1.8VS) FBVDDQ

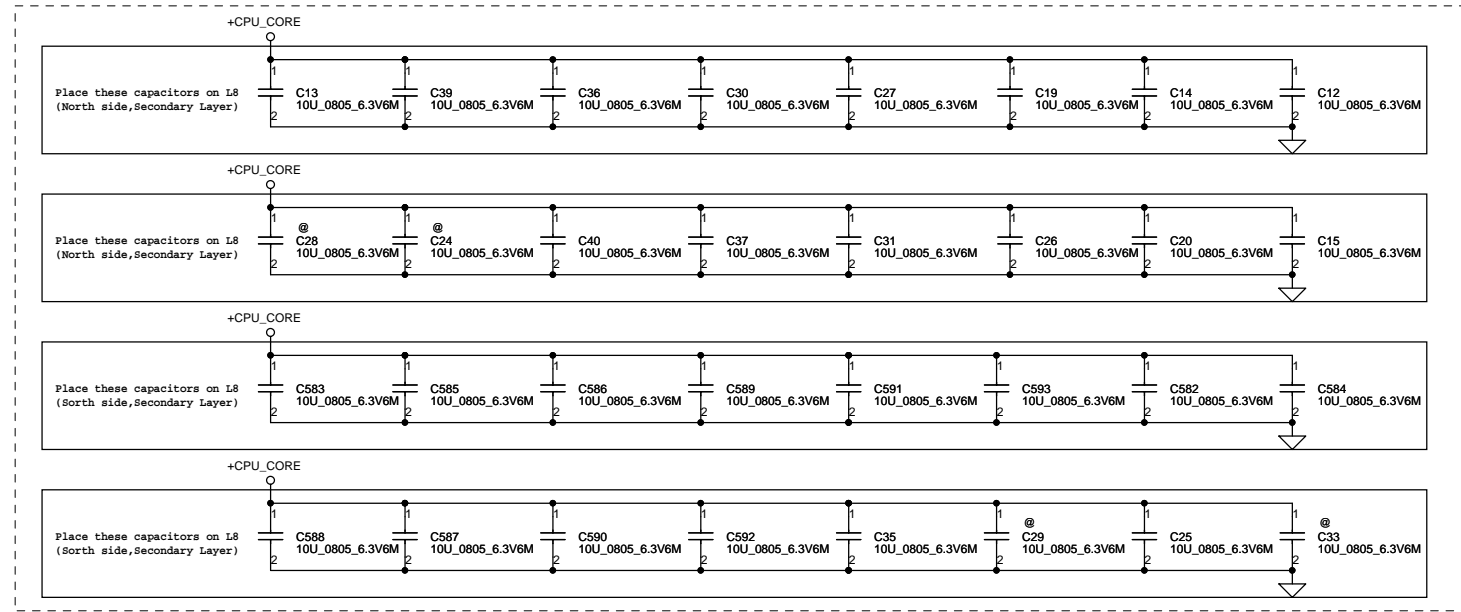
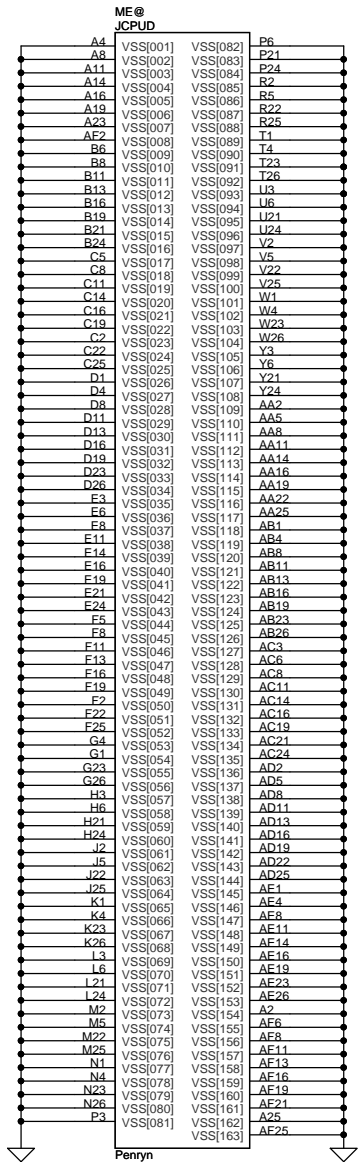


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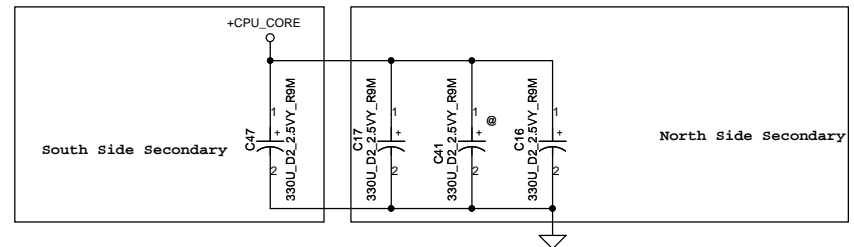


FAN1 Conn

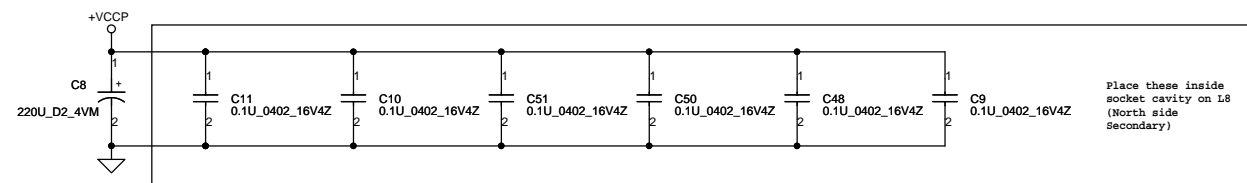
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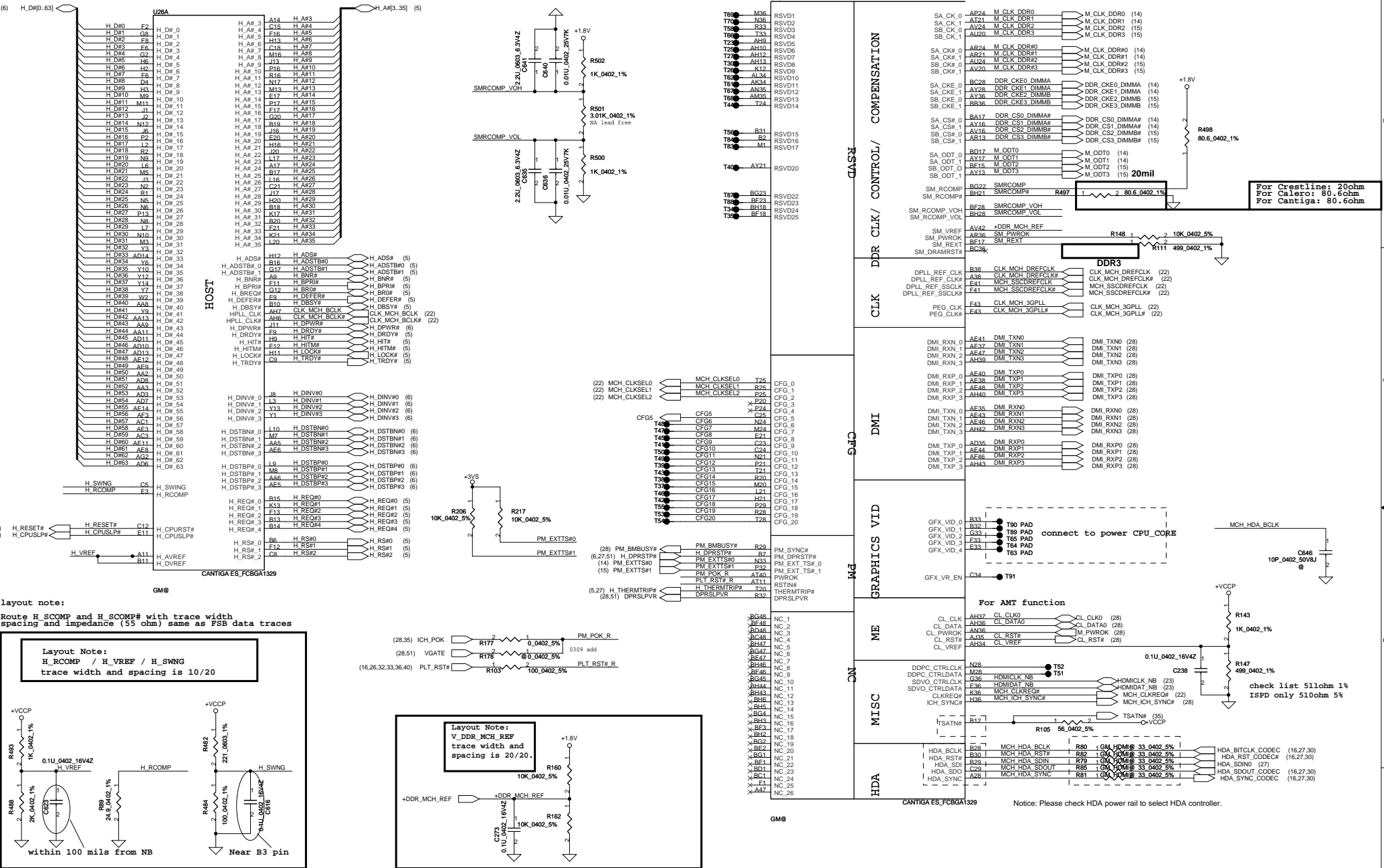
Mid Frequency Decoupling



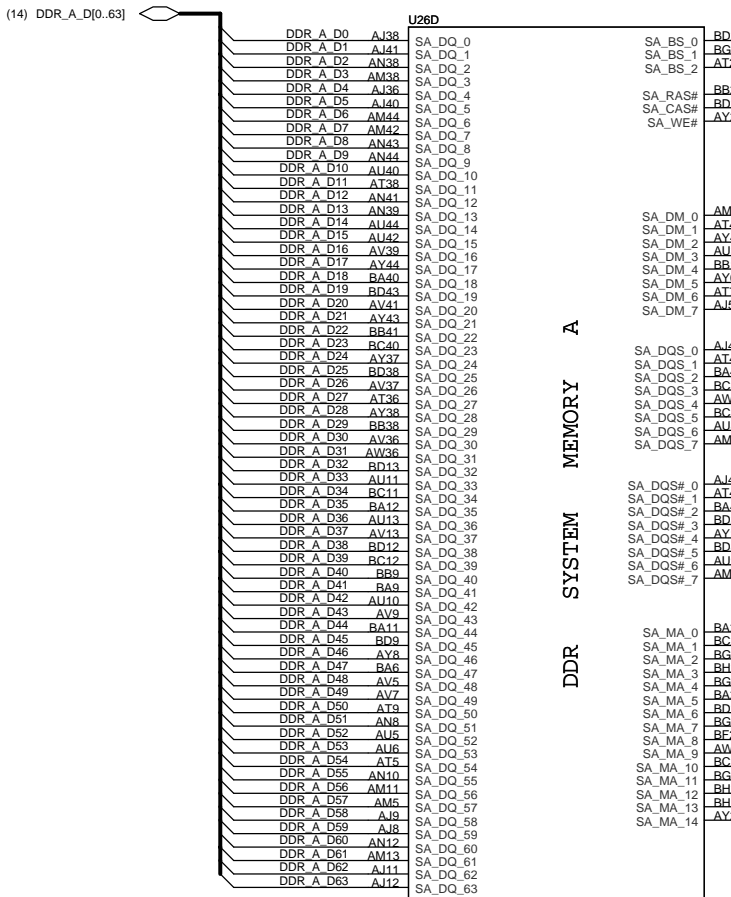
ESR <= 1.5m ohm
Capacitor > 1980uF



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(14) DDR_A_D[0..63]



A

DDR

SYSTEM

MEMORY

A

DDR

SYSTEM

MEMORY

A

DDR

SYSTEM

MEMORY

A

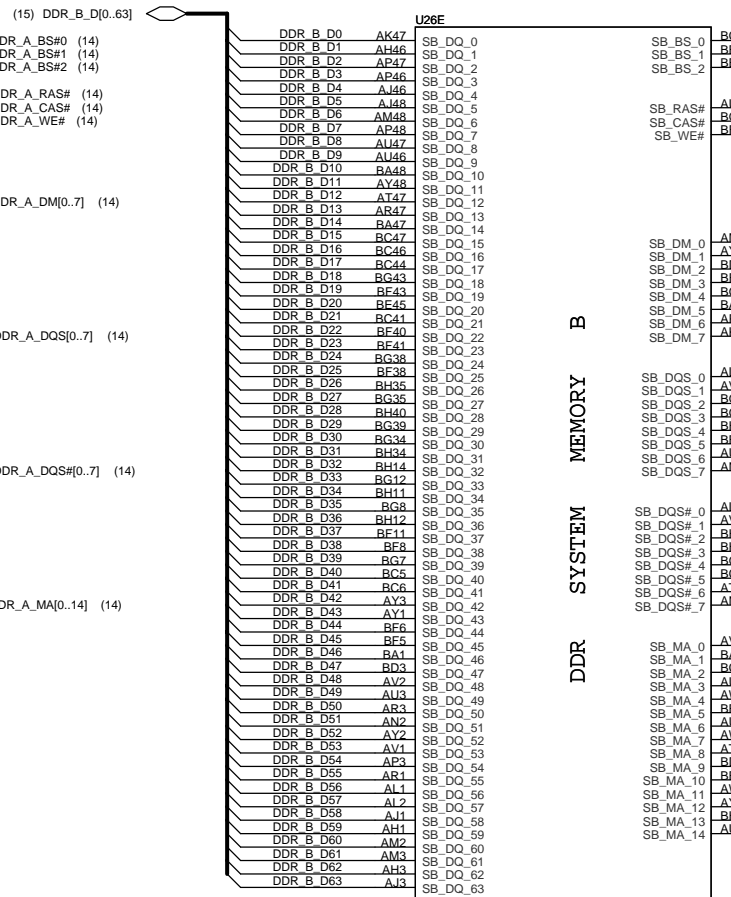
DDR

SYSTEM

MEMORY

A

(15) DDR_B_D[0..63]



B

DDR

SYSTEM

MEMORY

B

DDR

SYSTEM

MEMORY

B

DDR

SYSTEM

MEMORY

B

DDR

SYSTEM

MEMORY

B

CANTIGA ES_FCBGA1329

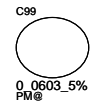
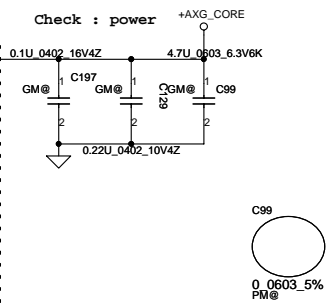
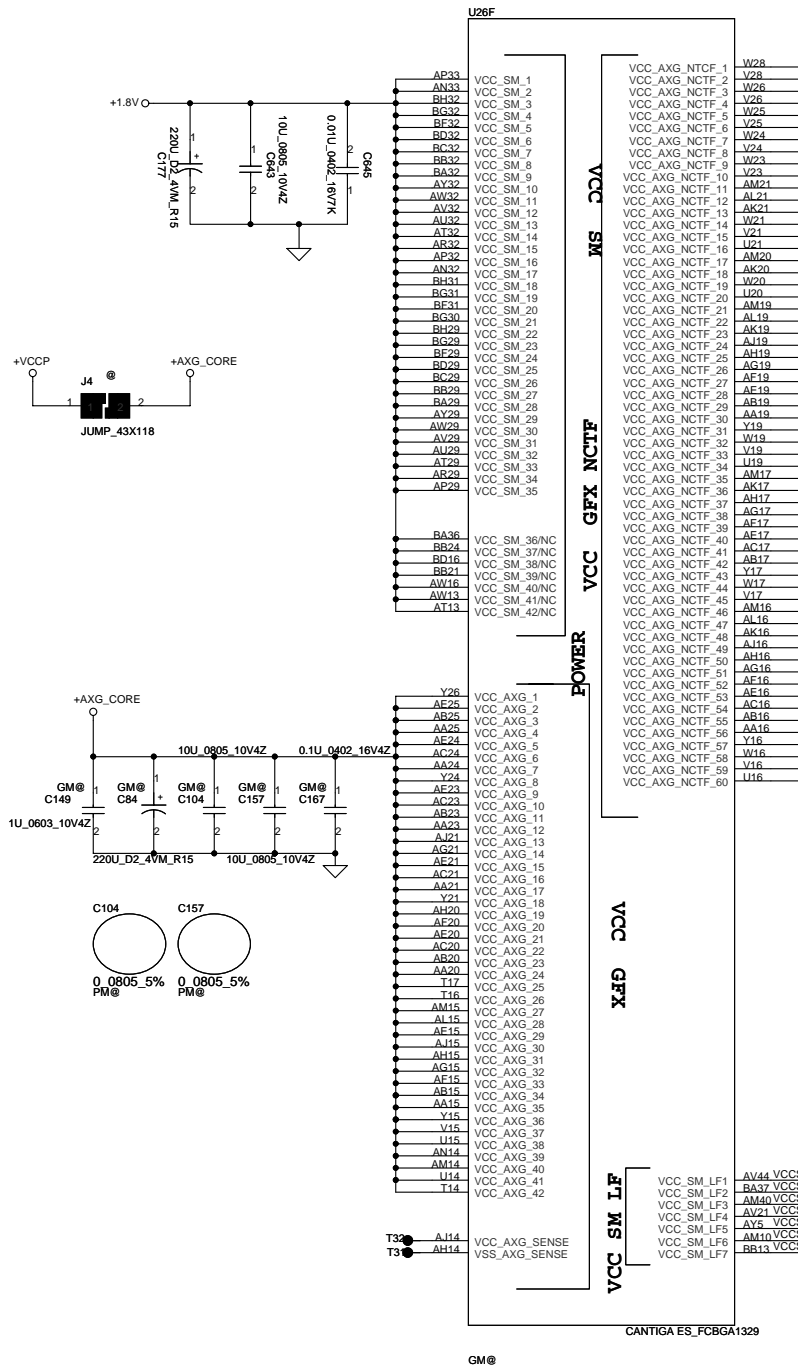
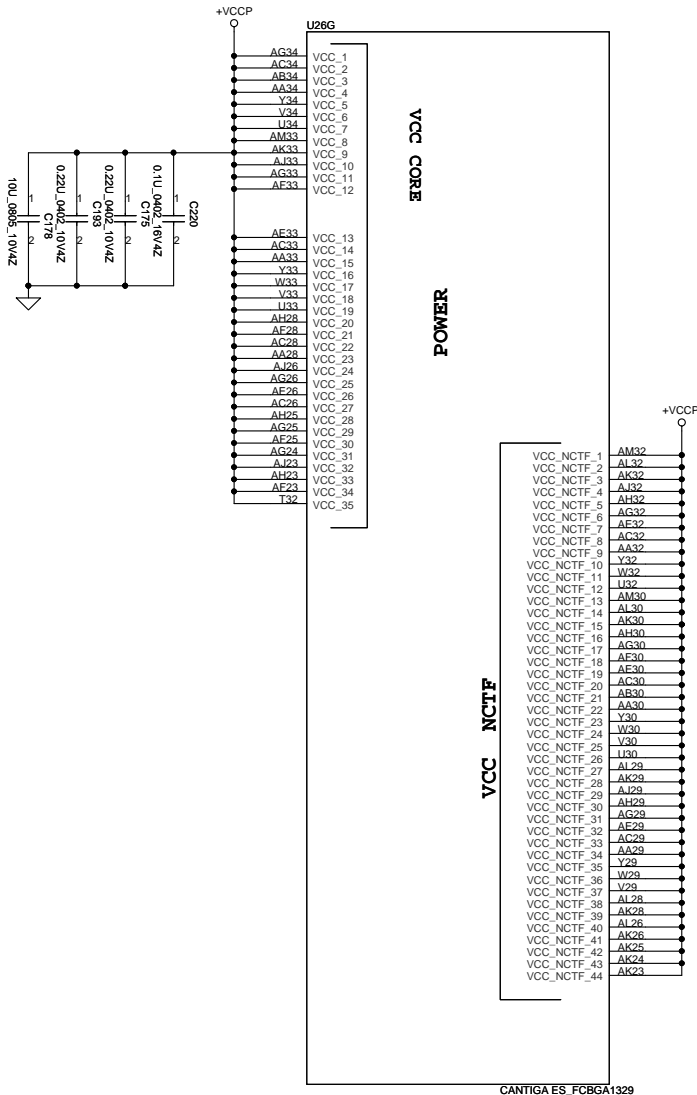
CANTIGA ES_FCBGA1329

GM@

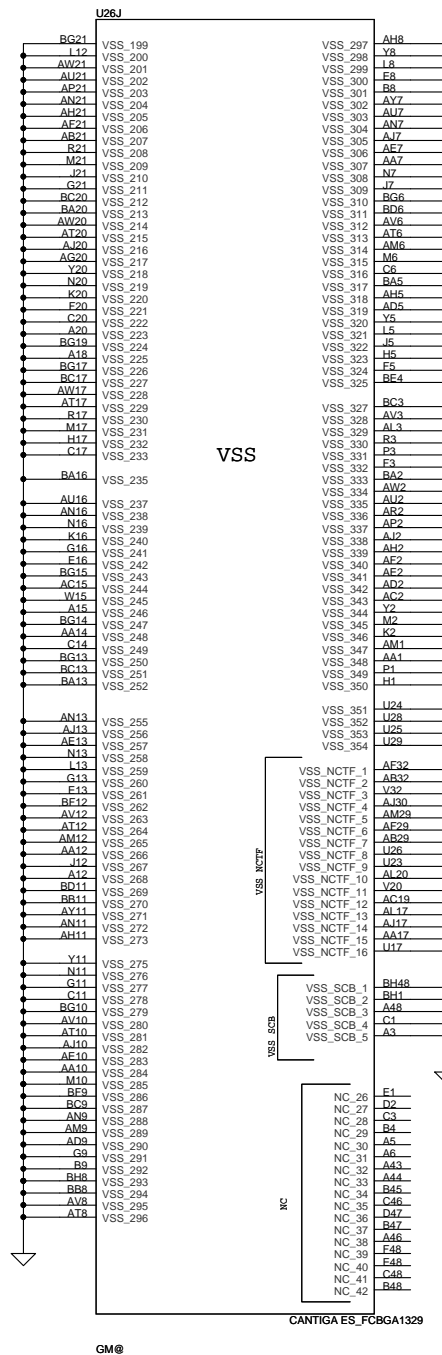
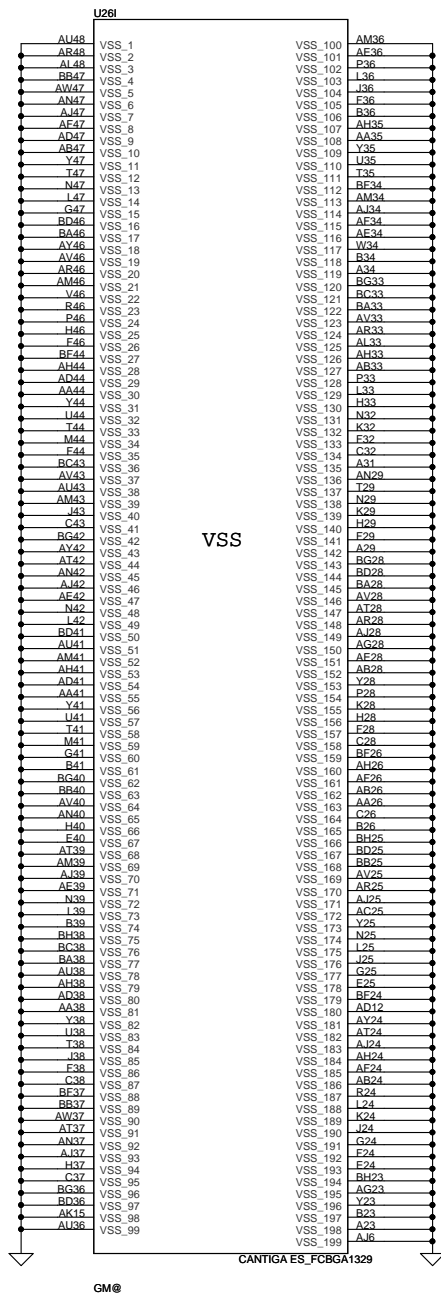
GM@

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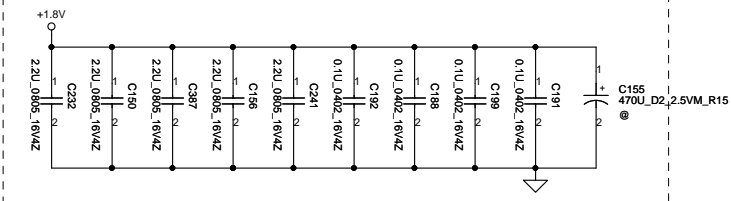
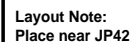
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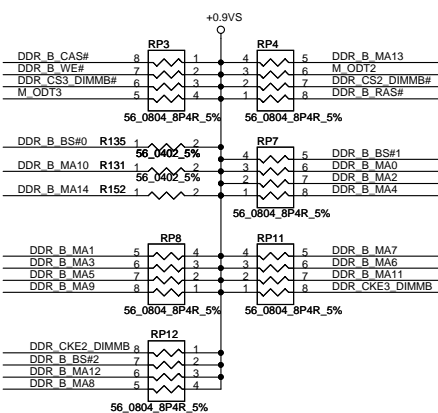
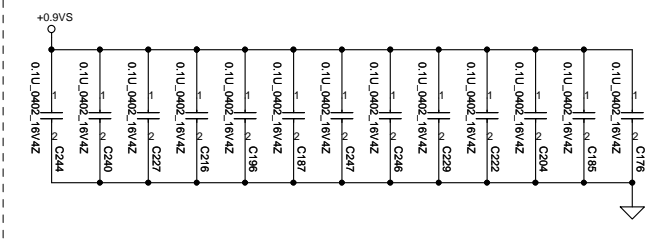
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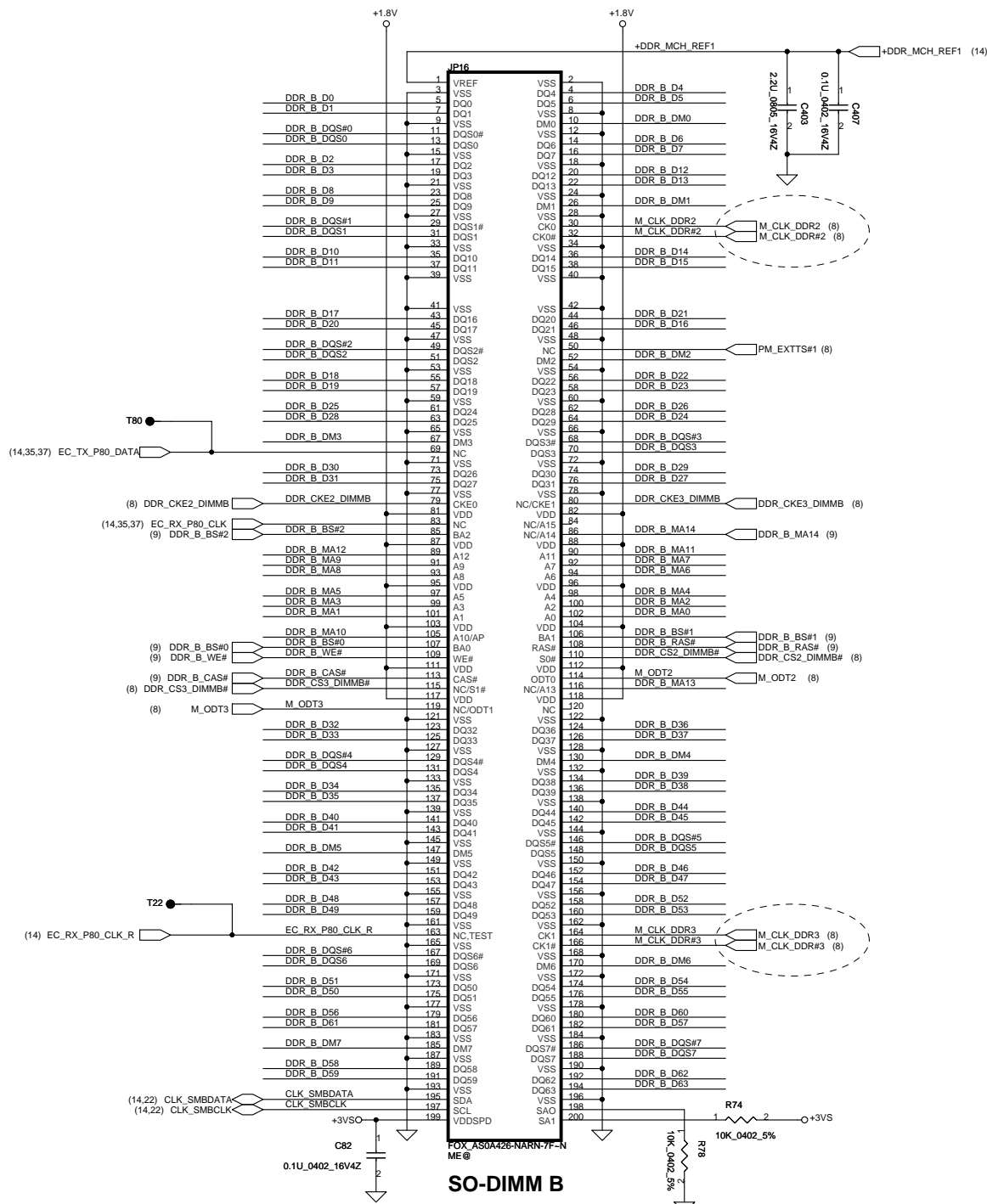
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Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor
closely JP42,all
trace length Max=1.5"



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(10) PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15]
(10) PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15]
(10) PCIE_GTX_C_MRX_N[0..15] PCIE_GTX_C_MRX_N[0..15]
(10) PCIE_GTX_C_MRX_P[0..15] PCIE_GTX_C_MRX_P[0..15]

PCIE_MTX_C_GRX_P0 AF12
PCIE_MTX_C_GRX_N0 AF12C
PCIE_MTX_C_GRX_P1 AG12
PCIE_MTX_C_GRX_N1 AG12C
PCIE_MTX_C_GRX_P2 AG13
PCIE_MTX_C_GRX_N2 AG13C
PCIE_MTX_C_GRX_P3 AE13
PCIE_MTX_C_GRX_N3 AE13C
PCIE_MTX_C_GRX_P4 AG14
PCIE_MTX_C_GRX_N4 AG14C
PCIE_MTX_C_GRX_P5 AE14
PCIE_MTX_C_GRX_N5 AE14C
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PCIE_MTX_C_GRX_N6 AG15C
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PCIE_MTX_C_GRX_P8 AE16
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PCIE_MTX_C_GRX_N12 AG19C
PCIE_MTX_C_GRX_P13 AE19
PCIE_MTX_C_GRX_N13 AE19C
PCIE_MTX_C_GRX_P14 AG20
PCIE_MTX_C_GRX_N14 AG20C
PCIE_MTX_C_GRX_P15 AE20
PCIE_MTX_C_GRX_N15 AE20C

Part 1 of 5

GPIO

DACA

DACB

DACC

PCI EXPRESS

I2C

TEST

CLK

HDA

GPIO0 N1
GPIO1 G1
GPIO2 C1
GPIO3 M2
GPIO4 M3
GPIO6 K3
GPIO6 K2
GPIO7 J2
GPIO8 M1
GPIO9 D2
GPIO10 D1
GPIO11 J1
GPIO12 J3
GPIO13 K1
GPIO14 F3
GPIO15 G2
GPIO16 G2
GPIO17 F1
GPIO18 F2
GPIO19 F2

DACA_HSYNC AD2
DACA_VSYNC AD1
DACA_RED AD2
DACA_BLUE AD3
DACA_GREEN AD3
DACA_VREF AE1
DACA_RSET AE1
DACB_CS D6
DACB_RED F7
DACB_BLUE F6
DACB_GREEN F7
DACB_VREF G6
DACB_RSET F8
DACC_HSYNC U6
DACC_VSYNC U4
DACC_RED U5
DACC_BLUE R4
DACC_GREEN T4
DACC_VREF R6
DACC_RSET V6

I2CA_SCL R1
I2CA_SDA T3
I2CB_SCL R2
I2CB_SDA R3
I2CC_SCL A2
I2CC_SDA B1
I2CD_SCL N2
I2CD_SDA N3
I2CE_SCL Y6
I2CE_SDA W6
I2CH_SCL A3
I2CH_SDA A4
I2CS_SCL T1
I2CS_SDA T2

VGA_DDCCLK_C R16
VGA_DDCDATA_C R17
VGA_ENVDV M3
VGA_ENBKL M3
VGA_HDMI_SCL Y6
VGA_HDMI_SDA W6
HDCP_SMB_CK1 A3
HDCP_SMB_DAI A4
EC_SMB_CK2 T1
EC_SMB_DAI2 T2

JTAG_TCK AE3
JTAG_TDI AG4
JTAG_TDO AE4
JTAG_TRST_N AG3
TESTMODE AD25

SPDIF_IN F9
VDD_SENSE W15
HDA_RST_N C6
HDA_SDI B6
HDA_SDO B6
HDA_SYNC_CODE R7
HDA_BITCLK_CODE R7

CRT OUT

+3VS

+3VS

EC_SMB_CK2 (5,35,41)

EC_SMB_DAI2 (5,35,41)

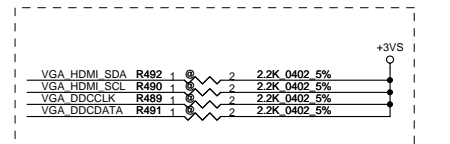
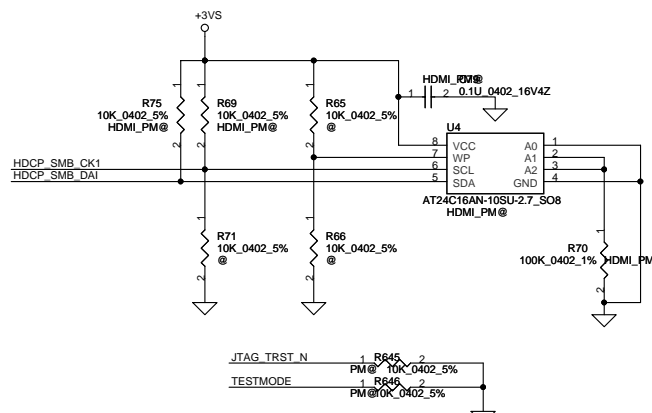
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HDA_SDI B6

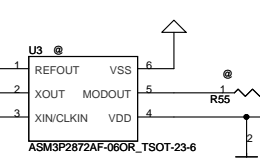
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HDA_SYNC_CODE R7

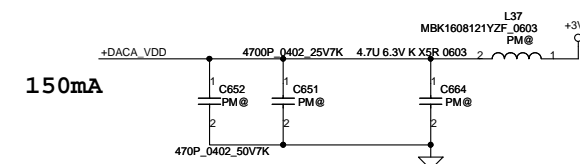
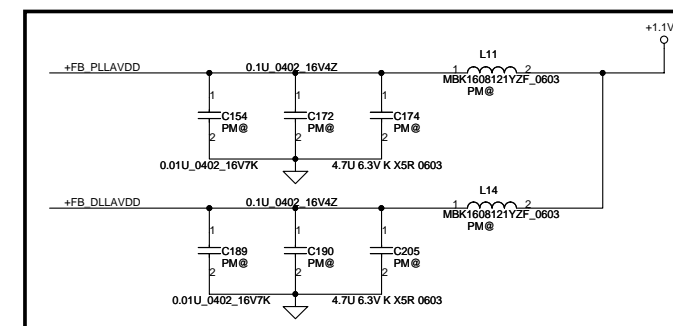
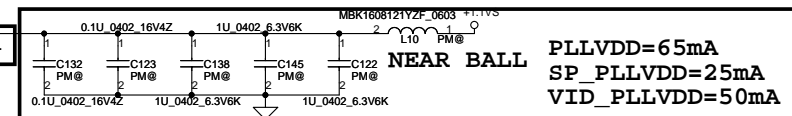
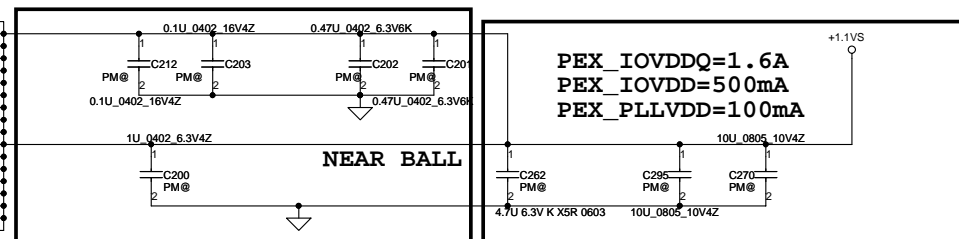
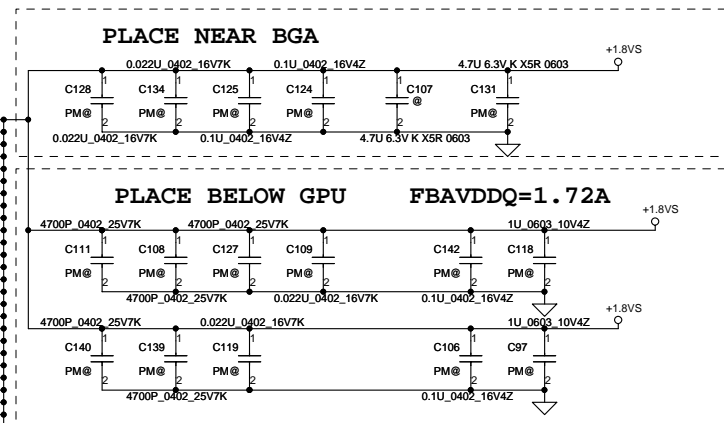
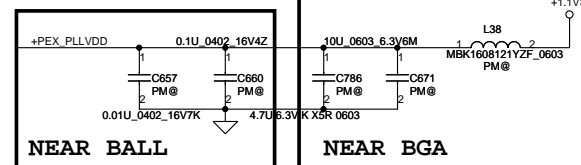
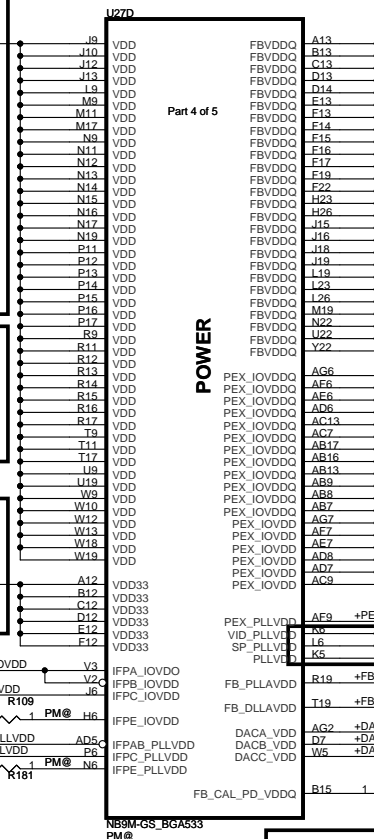
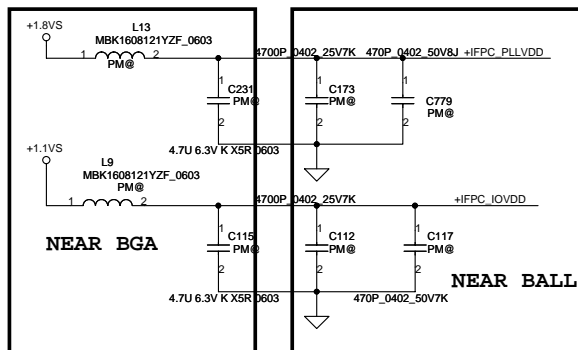
HDA_BITCLK_CODE R7



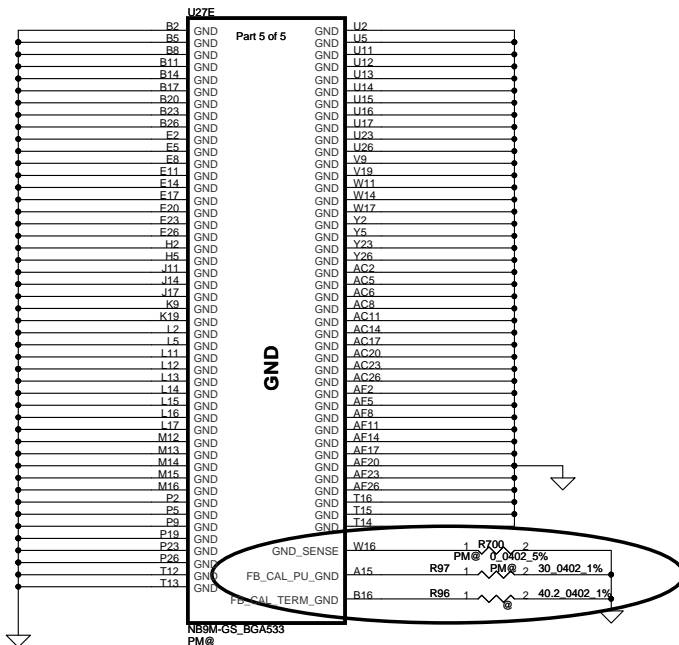
External Spread Spectrum



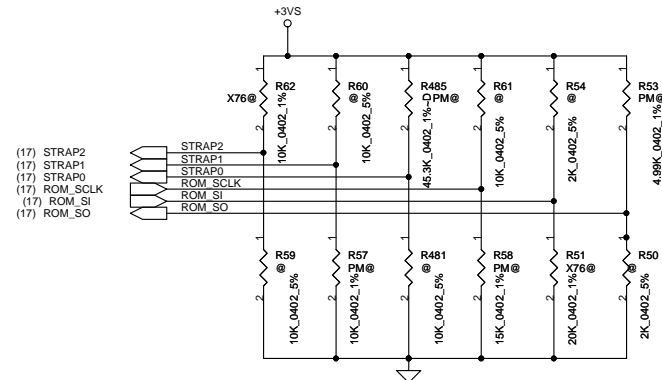
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A total of 8 signals are required for GB1 strapping this includes
 2 reference signals
 6 physical strapping pins
 4 logical strapping bits
 A total of 24 logical strapping bits are available



GB1 Family GPU Strap Options

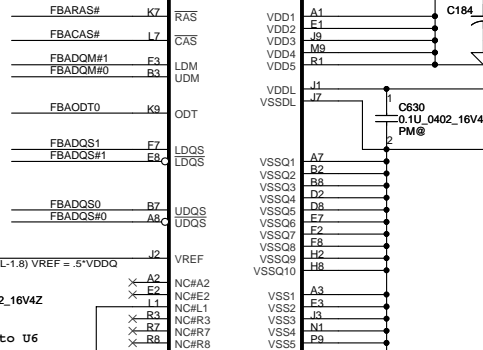
GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
NB9M-GS (0x06E9)	Samsung	16Mx16(1)	PU 5K	PD 15K	PD 10K	PU 10K	PD 45K
		32Mx16(5)	PU 5K	PD 15K	PD 30K	PU 10K	PD 45K
	Hynix	16Mx16(3)	PU 5K	PD 15K	PD 20K	PU 10K	PD 45K
		32Mx16(7)	PU 5K	PD 15K	PD 45K	PU 10K	PD 45K
	Qimonda	16Mx16(2)	PU 5K	PD 15K	PD 15K	PU 10K	PD 45K
		32Mx16(6)	PU 5K	PD 15K	PD 35K	PU 10K	PD 45K
NB9M-GE (0x06E8)	Samsung	16Mx16(1)	PU 5K	PD 15K	PD 10K	PU 5K	PD 45K
		32Mx16(5)	PU 5K	PD 15K	PD 30K	PU 5K	PD 45K
	Hynix	16Mx16(3)	PU 5K	PD 15K	PD 20K	PU 5K	PD 45K
		32Mx16(7)	PU 5K	PD 15K	PD 45K	PU 5K	PD 45K
	Qimonda	16Mx16(2)	PU 5K	PD 15K	PD 15K	PU 5K	PD 45K
		32Mx16(6)	PU 5K	PD 15K	PD 35K	PU 5K	PD 45K

Component	Manufacturer	Compal PN	Compal X76 PN
DDR2 VRAM (16M*16)	Hynix	SA000012G30	X7611338L01
	Qimonda	SA00001YF10	X7611338L02
	Samsung	SA00001KH10	X7611338L03
DDR2 VRAM (32M*16)	Hynix	SA00000FF30	X7611338L04
	Qimonda	SA00000S820	X7611338L05
	Samsung	SA00001VX10	X7611338L06

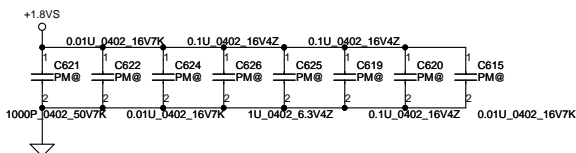
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FBA_BA0	L2	BA0	DQ15	B9	FBAD7
FBA_BA1	L3	BA1	DQ16	B1	FBAD3
			DQ17	D1	FBAD0
FBAA12	R2	A12	DQ18	D3	FBAD1
FBAA11	P7	A11	DQ19	D7	FBAD6
FBAA10	M2	A10/AP	DQ20	C2	FBAD2
FBAA9	P3	A9	DQ21	C8	FBAD5
FBAA8	P8	A8	DQ22	F9	FBAD10
FBAA7	P2	A7	DQ23	F1	FBAD15
FBAA6	N7	A6	DQ24	D6	FBAD8
FBAA5	N3	A5	DQ25	H9	FBAD9
FBAA4	N8	A4	DQ26	H1	FBAD12
FBAA3	N2	A3	DQ27	H3	FBAD11
FBAA2	M7	A2	DQ28	H7	FBAD14
FBAA1	M3	A1	DQ29	G2	FBAD11
FBAA0	M8	A0	DQ30	G8	FBAD11

FBACLK0#	K8	CK	VDDQ1	A9
FBACLK0	J8	CK	VDDQ2	C1
			VDDQ3	C3
FBA_CKE	K2	CKE	VDDQ4	C7
			VDDQ5	C9
			VDDQ6	E9
FBACS0#	L8	CS	VDDQ7	G1
FBAWE#	K3	WE	VDDQ8	G3
			VDDQ9	G7
			VDDQ10	G9
FBARAS#	K7	RAS	VDD1	A1
FBACAS#	L7	CAS	VDD2	E1
FBADQM#1	F3	LDM	VDD3	J9
FBADQM#0	B3	UDM	VDD4	M9
			VDD5	R1
FBAODT0	K9	ODT	VDDL	J1
			VSSDL	J7
FBADQS1	F7	LDQS	VSSQ1	A7
FBADQS#1	F8	LDQS	VSSQ2	B2
			VSSQ3	B8
			VSSQ4	D2
FBADQS0	B7	UDQS	VSSQ5	D8
FBADQS#0	A8	UDQS	VSSQ6	E7
			VSSQ7	F2
			VSSQ8	F8
			VSSQ9	H2
			VSSQ10	H8
			VSS1	A3
			VSS2	E3
			VSS3	J3
			VSS4	N1
			VSS5	P9

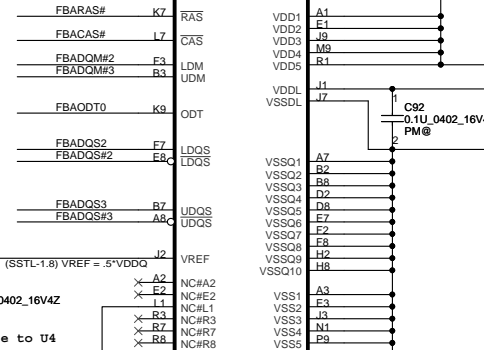


DDR2 BGA MEMORY

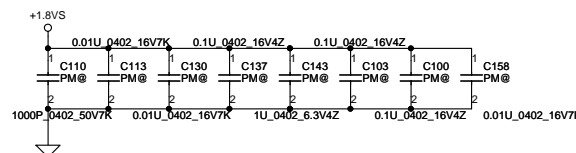


FBA_BA0	L2	BA0	DQ15	B9	FBAD25
FBA_BA1	L3	BA1	DQ16	B1	FBAD29
			DQ17	D1	FBAD24
FBAA12	R2	A12	DQ18	D3	FBAD28
FBAA11	P7	A11	DQ19	D7	FBAD27
FBAA10	M2	A10/AP	DQ20	C2	FBAD30
FBAA9	P3	A9	DQ21	C8	FBAD26
FBAA8	P8	A8	DQ22	F9	FBAD18
FBAA7	P2	A7	DQ23	F1	FBAD23
FBAA6	N7	A6	DQ24	D6	FBAD17
FBAA5	N3	A5	DQ25	H9	FBAD21
FBAA4	N8	A4	DQ26	H1	FBAD19
FBAA3	N2	A3	DQ27	H3	FBAD16
FBAA2	M7	A2	DQ28	G2	FBAD22
FBAA1	M3	A1	DQ29	G8	FBAD20
FBAA0	M8	A0	DQ30		

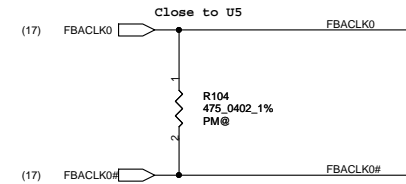
FBACLK0#	K8	CK	VDDQ1	A9
FBACLK0	J8	CK	VDDQ2	C1
			VDDQ3	C3
FBA_CKE	K2	CKE	VDDQ4	C7
			VDDQ5	C9
			VDDQ6	E9
FBACS0#	L8	CS	VDDQ7	G1
FBAWE#	K3	WE	VDDQ8	G3
			VDDQ9	G7
			VDDQ10	G9
FBARAS#	K7	RAS	VDD1	A1
FBACAS#	L7	CAS	VDD2	E1
FBADQM#2	F3	LDM	VDD3	J9
FBADQM#3	B3	UDM	VDD4	M9
			VDD5	R1
FBAODT0	K9	ODT	VDDL	J1
			VSSDL	J7
FBADQS2	F7	LDQS	VSSQ1	A7
FBADQS#2	F8	LDQS	VSSQ2	B2
			VSSQ3	B8
			VSSQ4	D2
FBADQS3	B7	UDQS	VSSQ5	D8
FBADQS#3	A8	UDQS	VSSQ6	E7
			VSSQ7	F2
			VSSQ8	F8
			VSSQ9	H2
			VSSQ10	H8
			VSS1	A3
			VSS2	E3
			VSS3	J3
			VSS4	N1
			VSS5	P9



DDR2 BGA MEMORY

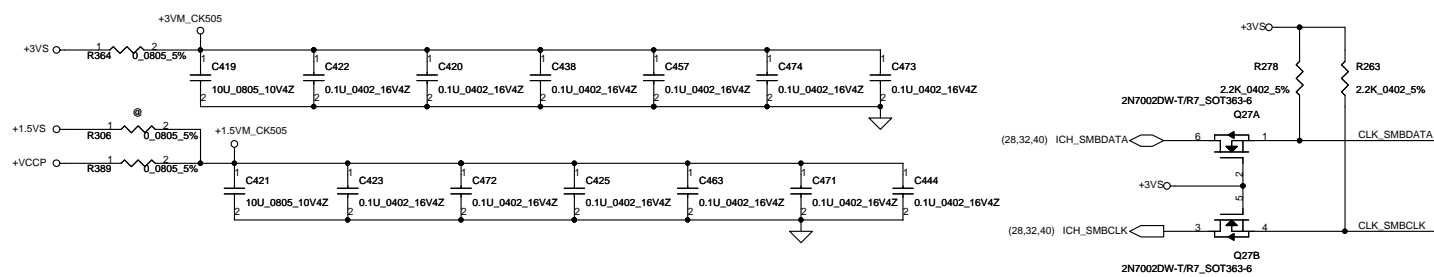


- (17,21) FBBA[2..5] FBBA[2..5]
- (17,21) FBAD[0..63] FBAD[0..63]
- (17,21) FBAA[0..12] FBAA[0..12]
- (17,21) FBADQS[0..7] FBADQS[0..7]
- (17,21) FBADQS#[0..7] FBADQS#[0..7]
- (17,21) FBADQM#[0..7] FBADQM#[0..7]
- (17,21) FBA_BA0 FBA_BA0
- (17,21) FBA_BA1 FBA_BA1
- (17,21) FBAODT0 FBAODT0
- (17,21) FBA_CKE FBA_CKE
- (17,21) FBARAS# FBARAS#
- (17,21) FBACAS# FBACAS#
- (17,21) FBAWE# FBAWE#
- (17,21) FBACS0# FBACS0#

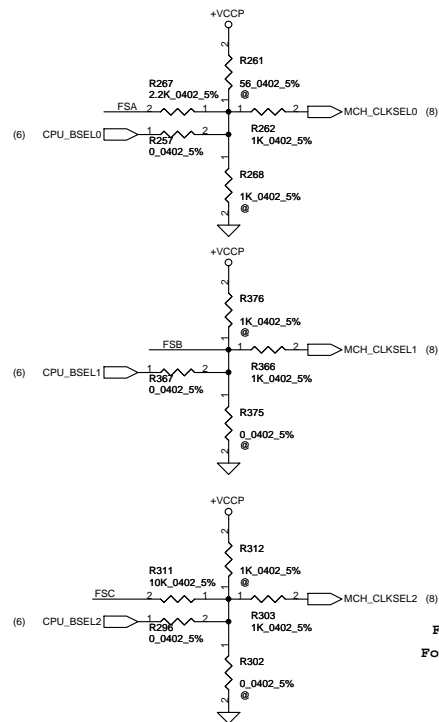


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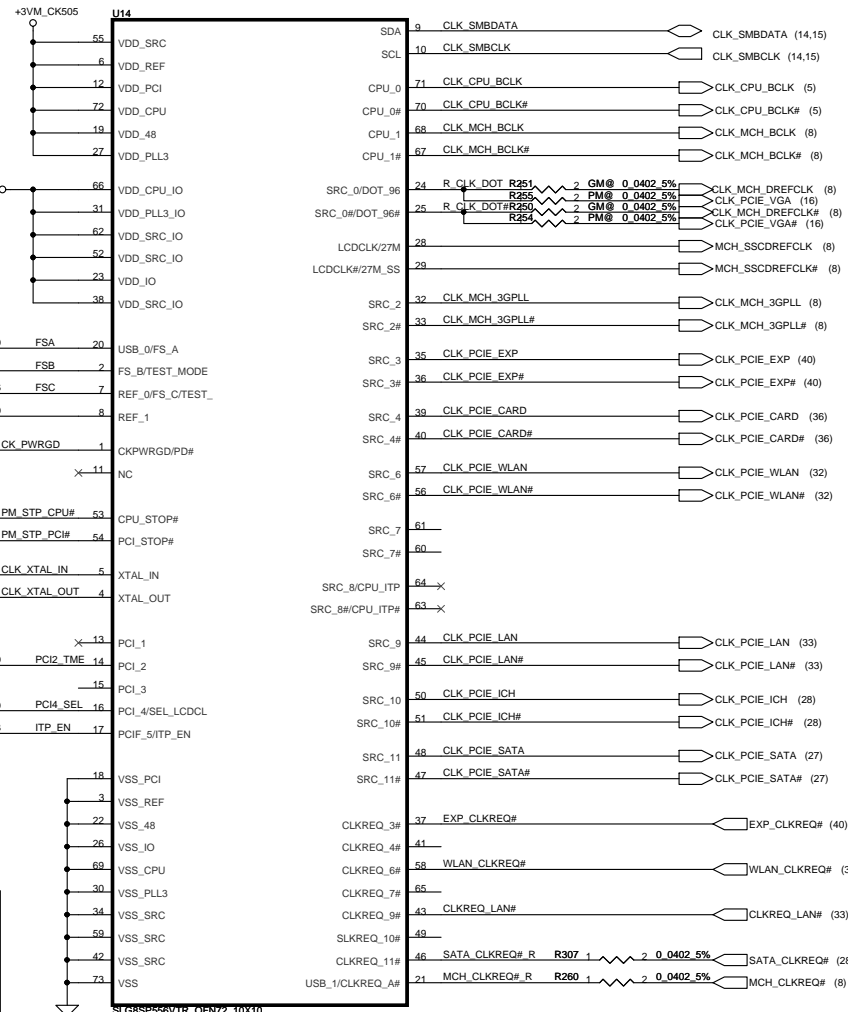
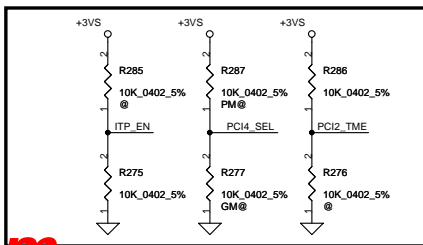
FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



SA000020K00 (Silego : SLG8SP556VTR)
SA000020H00 (ICS : ICS9LPRS387AKLFT)



For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS



SRC PORT LIST

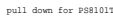
PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	
SRC6	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

SATA_CLKREQ# R315 2 1 10K_0402_5%
EXP_CLKREQ# R295 2 1 10K_0402_5%
MCH_CLKREQ# R256 2 1 10K_0402_5%
CLKREQ_LAN# R304 2 1 10K_0402_5%
WLAN_CLKREQ# R372 2 1 10K_0402_5%

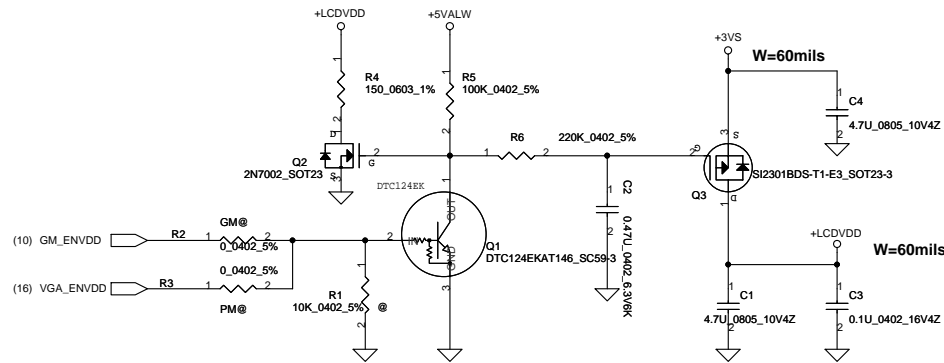
REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

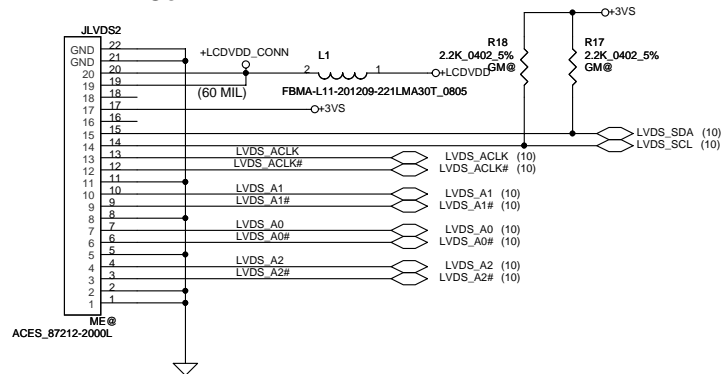
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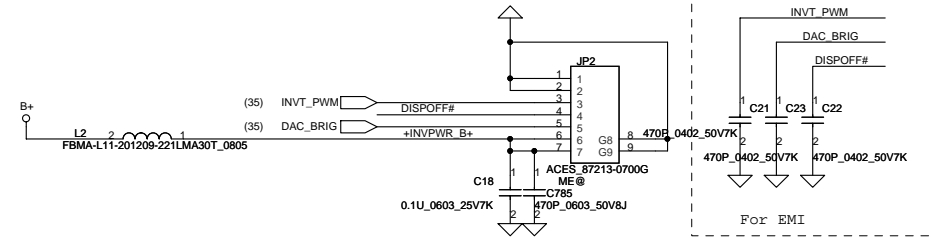
LCD POWER CIRCUIT



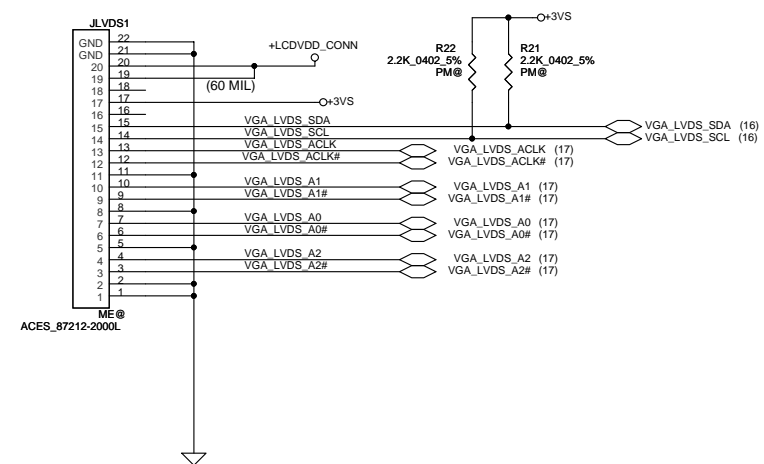
LCD/PANEL BD. Conn.



INVERTER Conn.

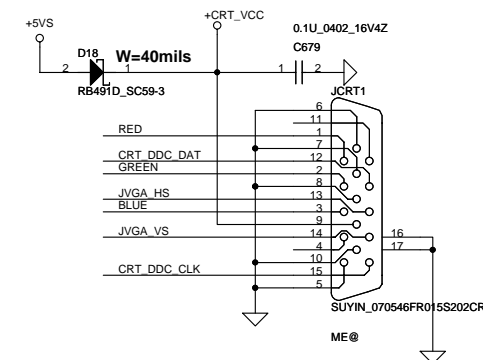


LCD/PANEL BD. Conn.



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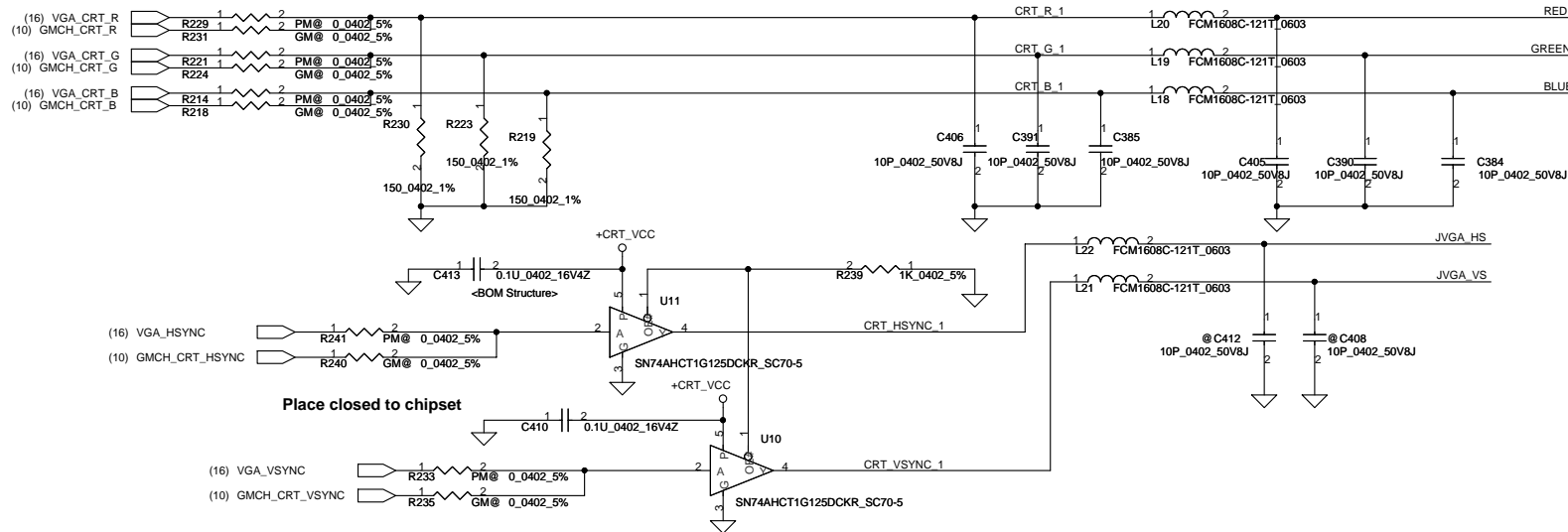
CRT Connector



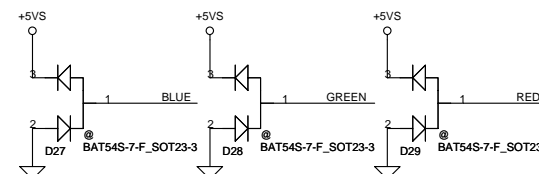
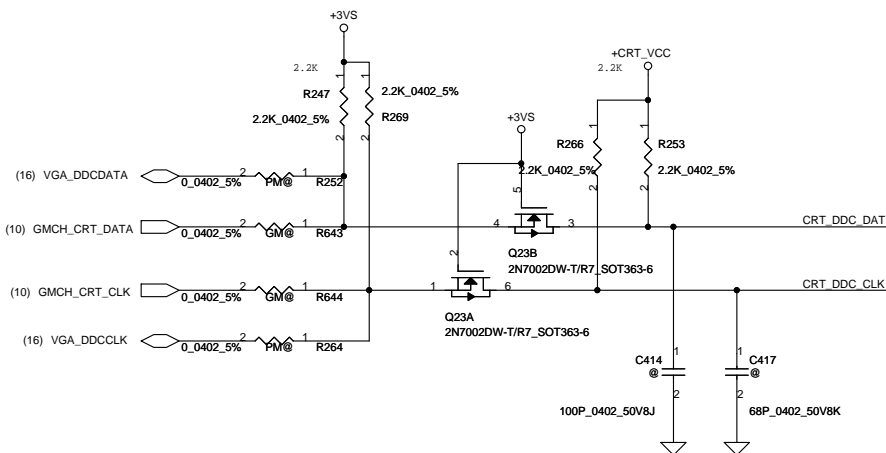
PIN ASSIGNMENT

D-SUB	FUNCTION
9	+CRT_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VSYNC
10	GND
13	HSYNC
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4

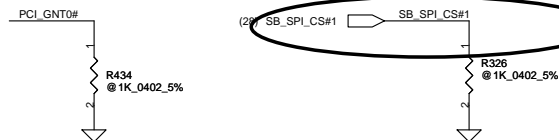
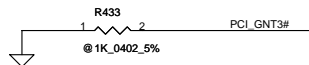
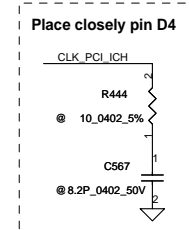
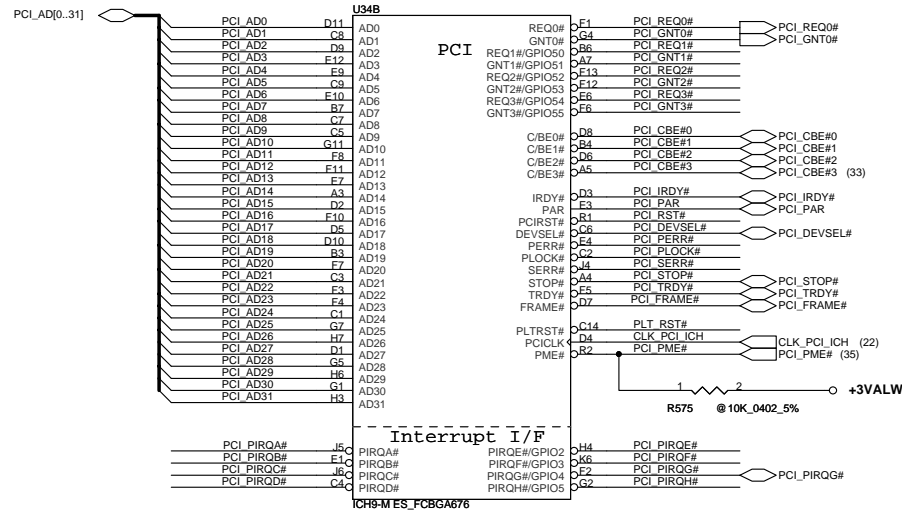
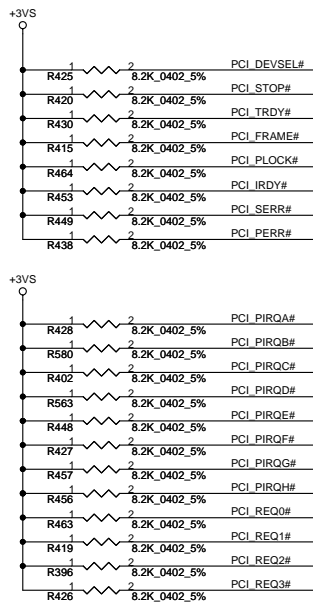
Place closed to chipset



Place closed to chipset



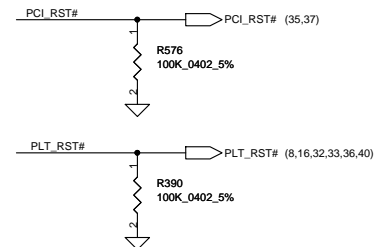
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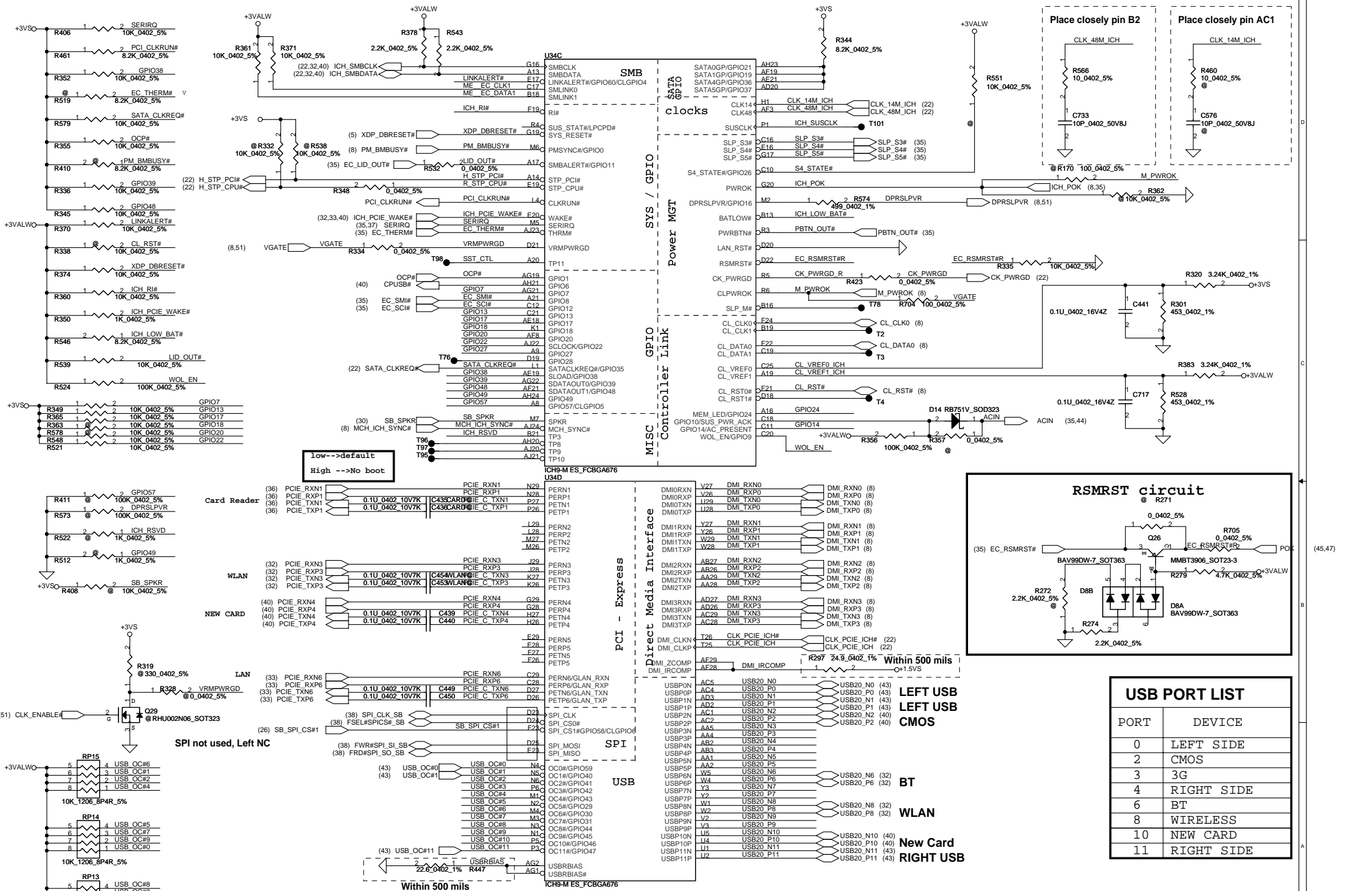


Pull high?

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

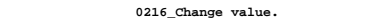




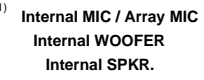


0308_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680p

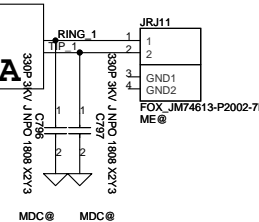
For Layout:
Place decoupling caps near the power pins of SmartAMC device.



(3.33V)
250mW



Place these C and R around AGND and DGND,
then choose the one which is close to Codec

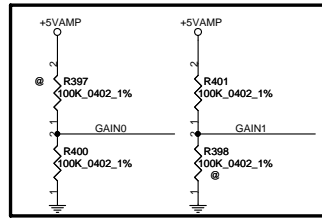


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				Custom	401557	1
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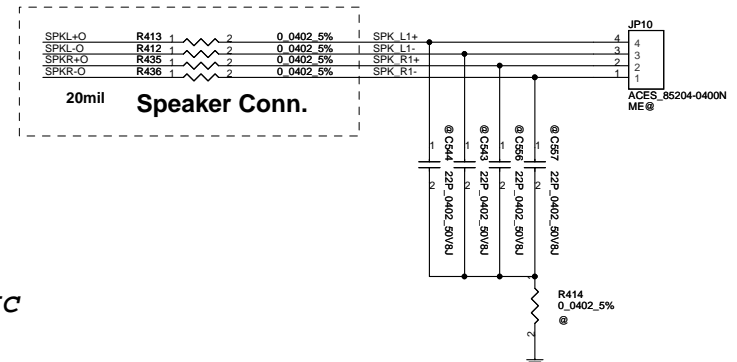
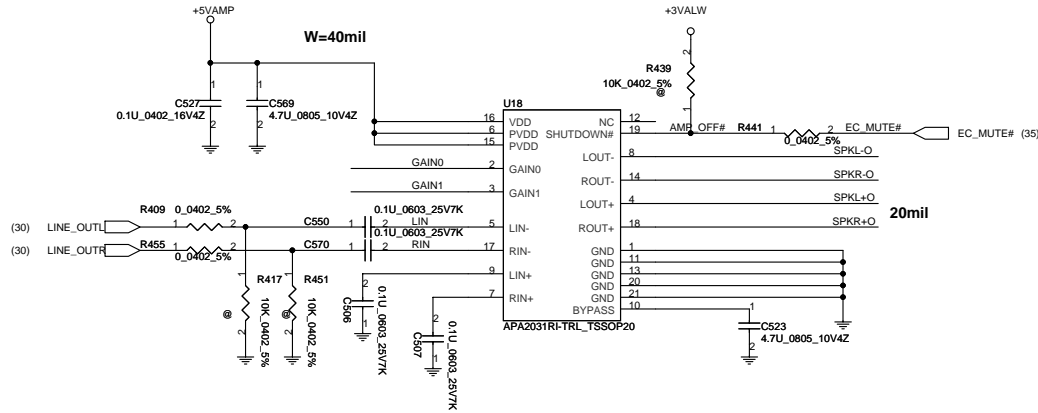
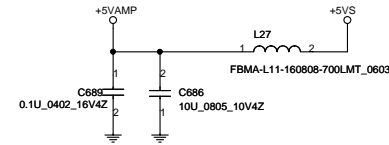
Speaker Amplifier

1nd = TPA6017 (SA601720010)

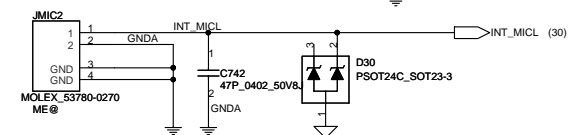
2nd = APA2031 (SA00001RZ00)



GAIN0	GAIN1	Gain
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



INT MIC



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Date: Saturday, June 06, 2009				Sheet 31 of 53

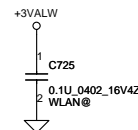
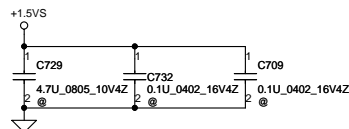
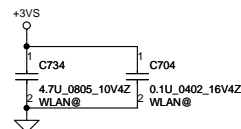
Compal Electronics, Inc.

SCHEMATIC, M/B LA-4211P

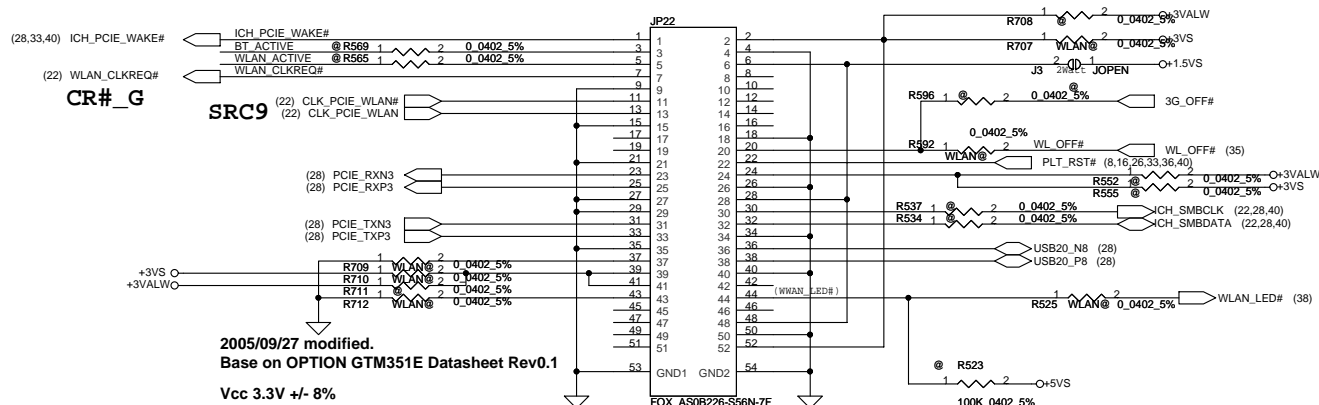
Rev 1

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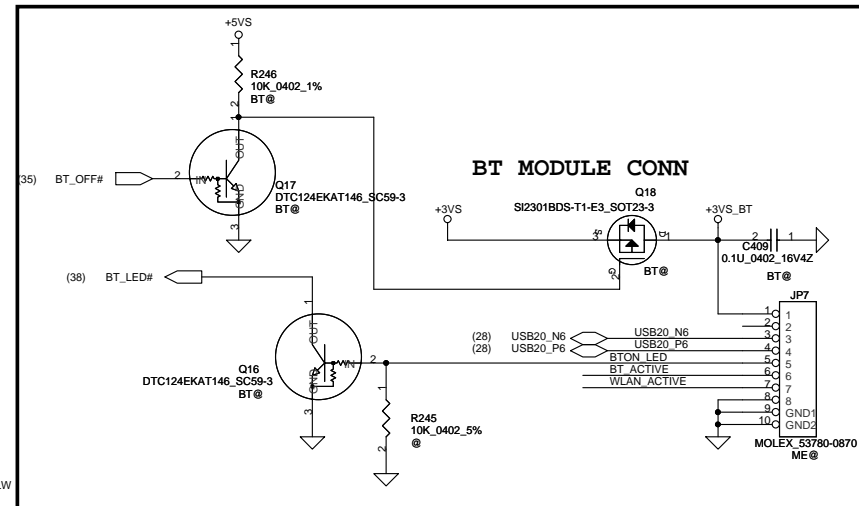
Mini-Express Card for 3G Or TV Tuner Mini-Express Card for WLAN



Mini-Express Card(Slot 1-WLAN)

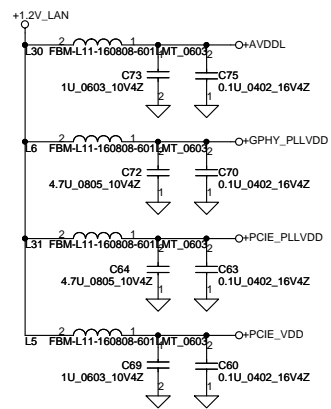
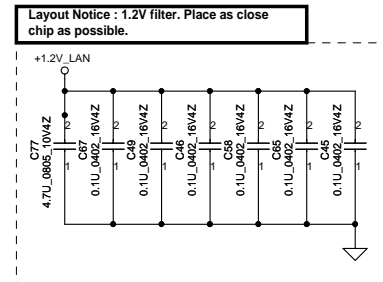
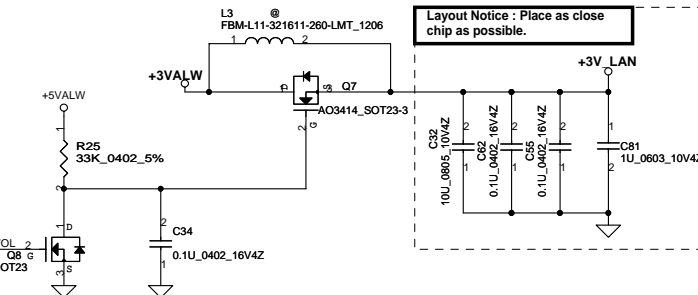
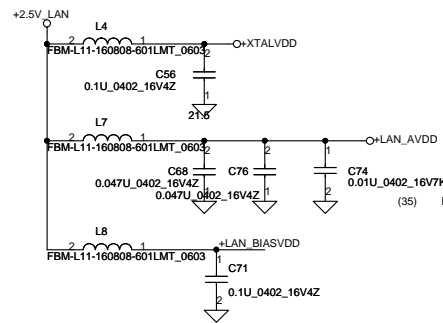


2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

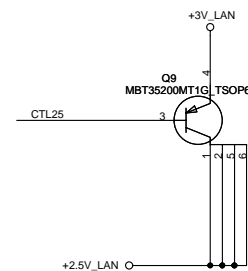
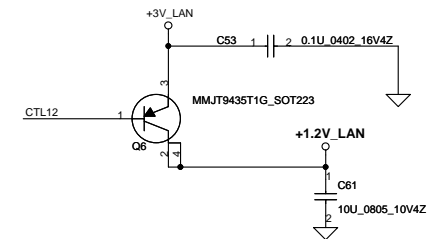
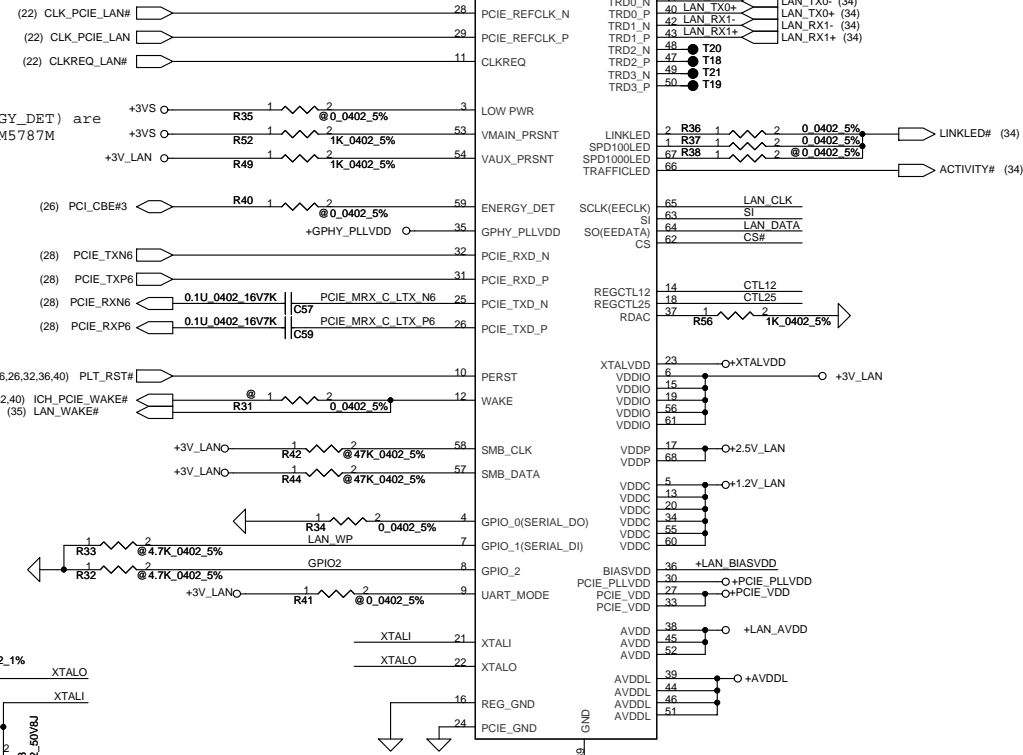


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					401557
				Date:	Saturday, June 06, 2009
				Sheet	32 of 53
				Rev	1

Layout Notice : Filter place as close chip as possible.

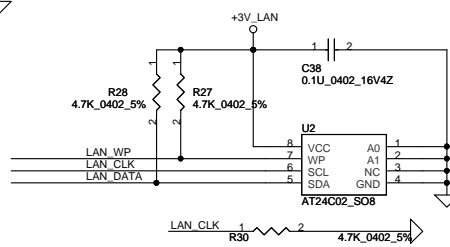
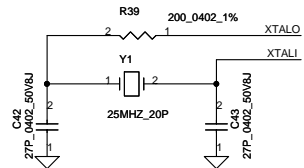
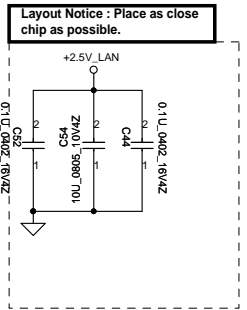


(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M



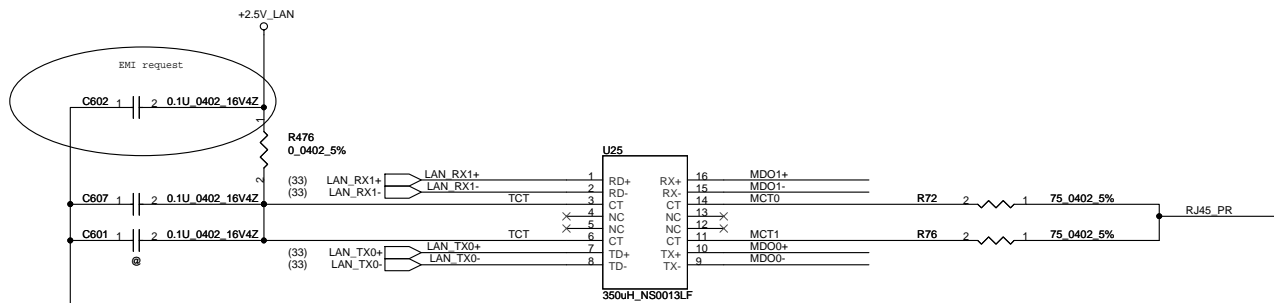
Notice : 4.7u 6.3V capactor Thickness 1.25mm

Layout Notice : Filter place as close chip as possible.

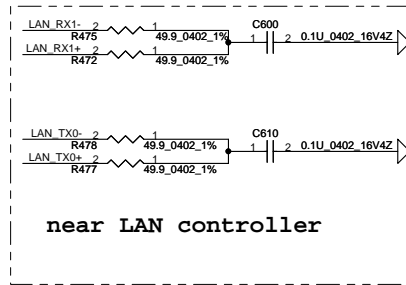


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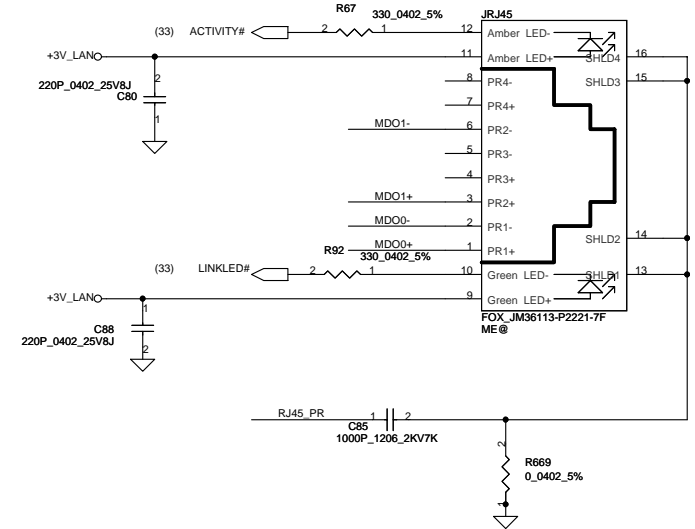
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Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF

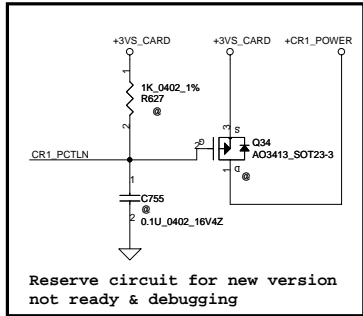


RJ45 CONN

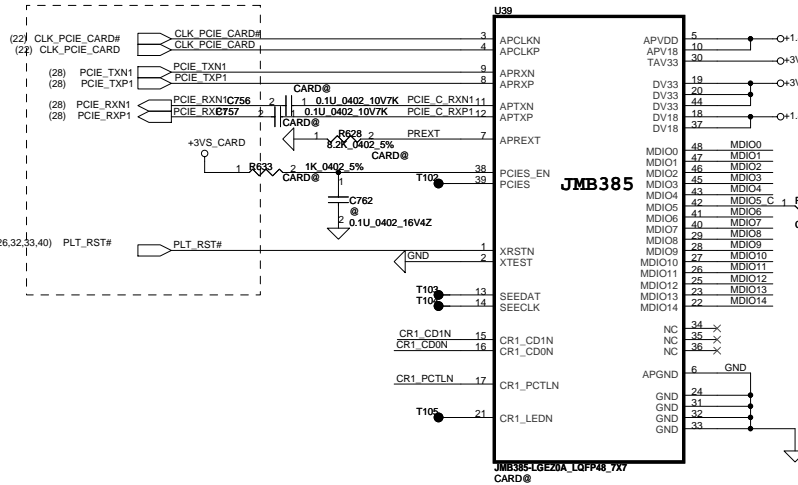


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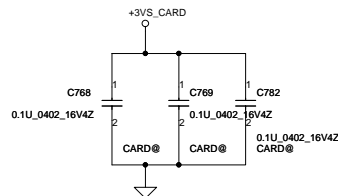
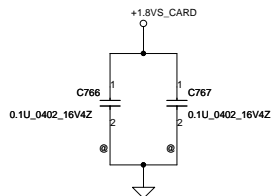
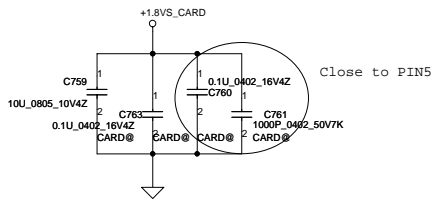
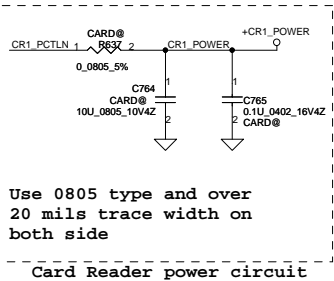
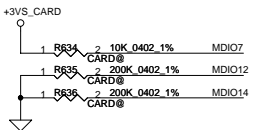
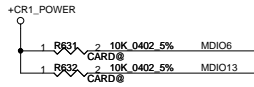


Need check CLK GEN &
SB select pin & page



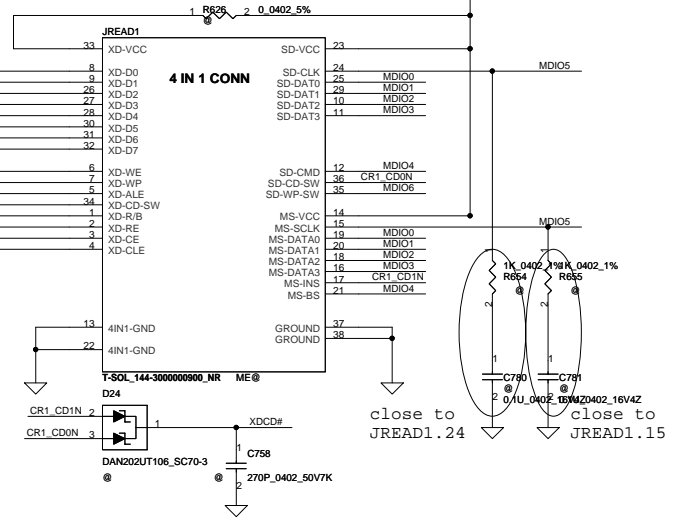
JMB385 Operation Modes

	Normal
XTEST	0
CR1_CD0N	X
CR1_CD1N	X



MDIO0	0	R671	2	0.0402 5%
MDIO1	0	R672	2	0.0402 5%
MDIO2	0	R673	2	0.0402 5%
MDIO3	0	R674	2	0.0402 5%
MDIO4	0	R675	2	0.0402 5%
MDIO5	0	R676	2	0.0402 5%
MDIO6	0	R677	2	0.0402 5%
MDIO7	0	R678	2	0.0402 5%
MDIO8	0	R679	2	0.0402 5%
MDIO9	0	R680	2	0.0402 5%
MDIO10	0	R681	2	0.0402 5%
MDIO11	0	R682	2	0.0402 5%

MDIO4	0	R679	2	0.0402 5%
MDIO5	0	R680	2	0.0402 5%
MDIO6	0	R681	2	0.0402 5%
MDIO7	0	R682	2	0.0402 5%
MDIO8	0	R683	2	0.0402 5%
MDIO9	0	R684	2	0.0402 5%
MDIO10	0	R685	2	0.0402 5%
MDIO11	0	R686	2	0.0402 5%
MDIO12	0	R687	2	0.0402 5%
MDIO13	0	R688	2	0.0402 5%
MDIO14	0	R689	2	0.0402 5%

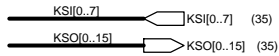


SD,MMC,MS,XD multi-function pin define

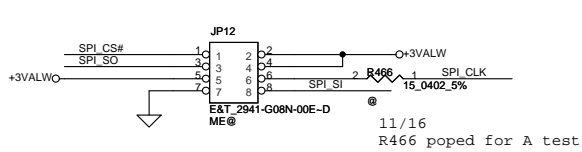
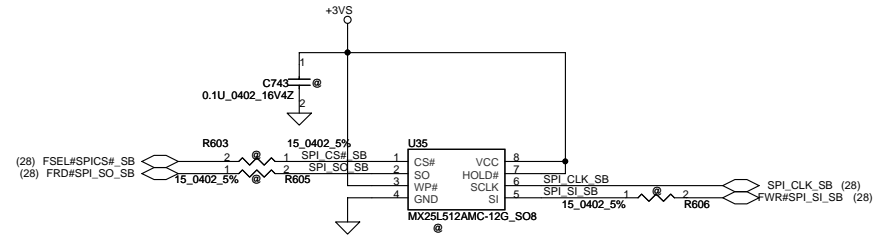
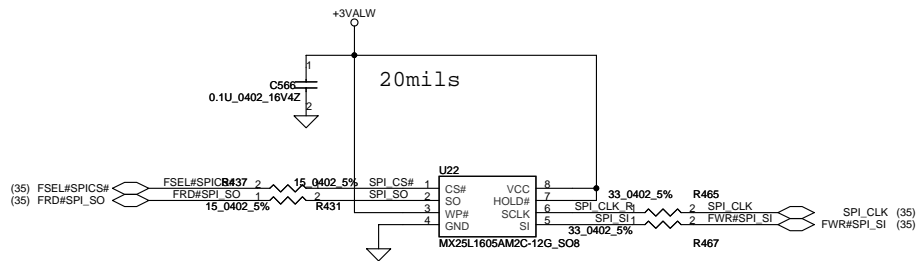
MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SD_DAT0	MMC_DAT0	MS_DAT0	XD_DAT0
MDIO01	SD_DAT1	MMC_DAT1	MS_DAT1	XD_DAT1
MDIO02	SD_DAT2	MMC_DAT2	MS_DAT2	XD_DAT2
MDIO03	SD_DAT3	MMC_DAT3	MS_DAT3	XD_DAT3
MDIO04	SD_CMD	MMC_CMD	MS_BS	XD_WE#
MDIO05	SDCLK1	MMCCLK	MSCCLK	XD_CE#
MDIO06	SD_WP#	MMC_WP#		XD_WP#
MDIO07				XD_CLE
MDIO08		MMC_DAT4	MS_DAT4	XD_DAT4
MDIO09		MMC_DAT5	MS_DAT5	XD_DAT5
MDIO10		MMC_DAT6	MS_DAT6	XD_DAT6
MDIO11		MMC_DAT7	MS_DAT7	XD_DAT7
MDIO12				XD_RE#
MDIO13				XD_R/B#
MDIO14				XD_ALE

Cardreader contactor not support MMC & MS
Bit 4~7

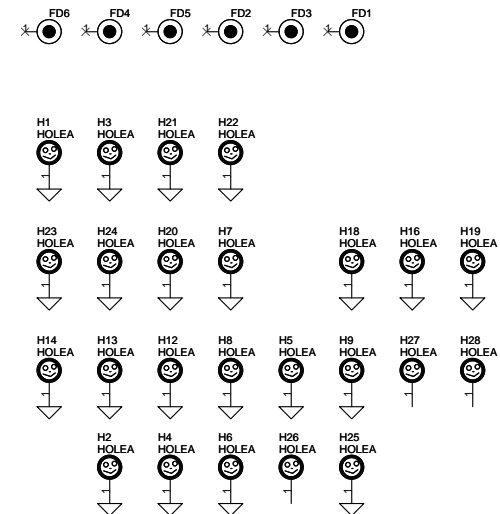
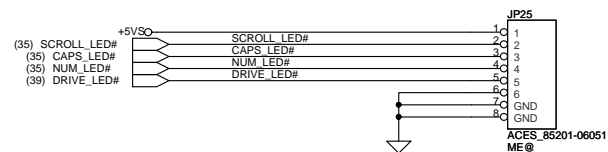
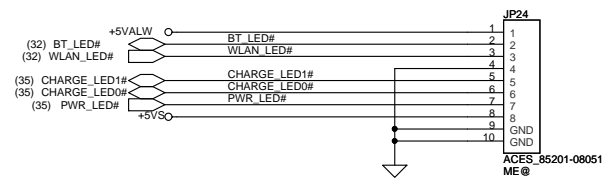
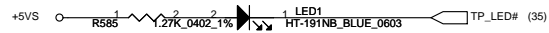
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FOR EC 8M SPI ROM

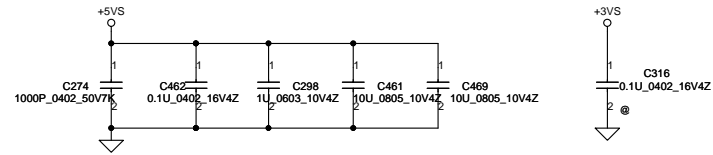


LED



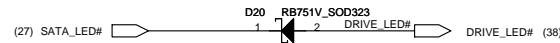
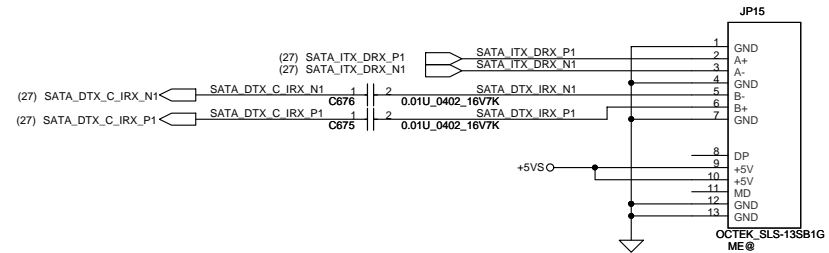
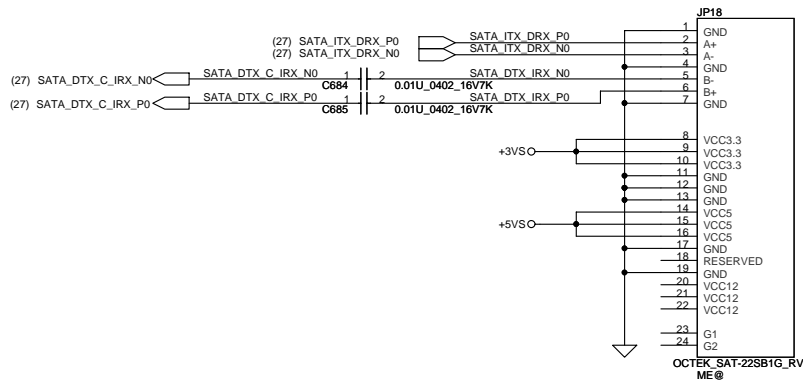
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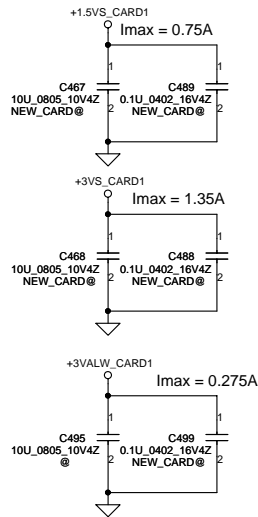
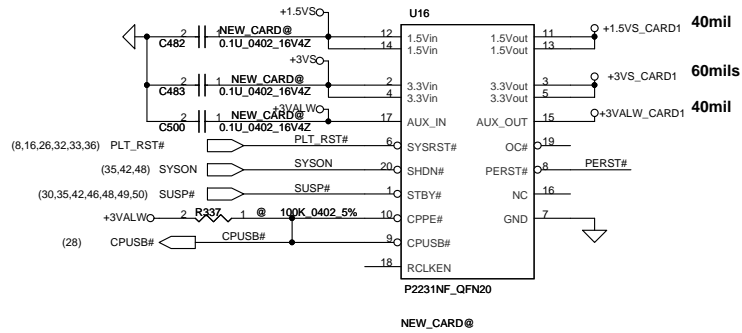
SATA HDD Conn.

SATA ODD Conn.

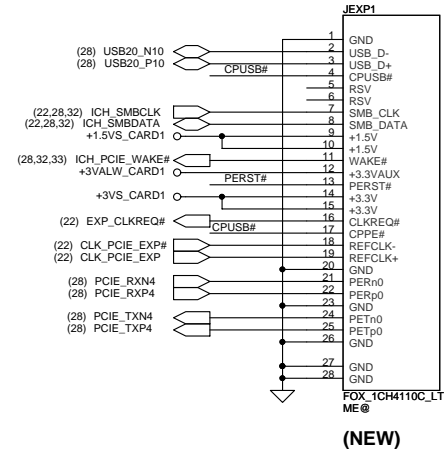


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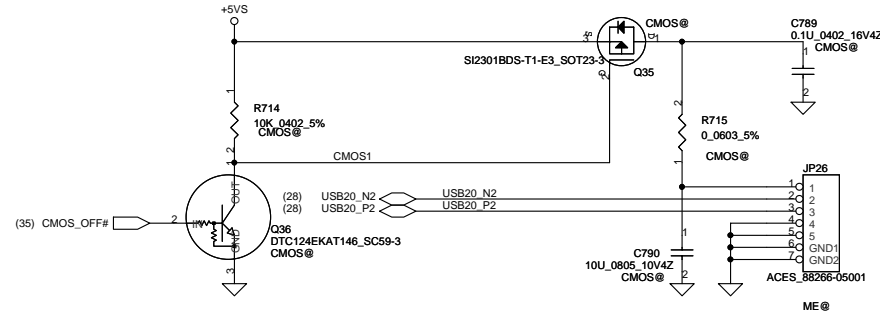
Express Card Power Switch



New Card Socket (Left/TOP)



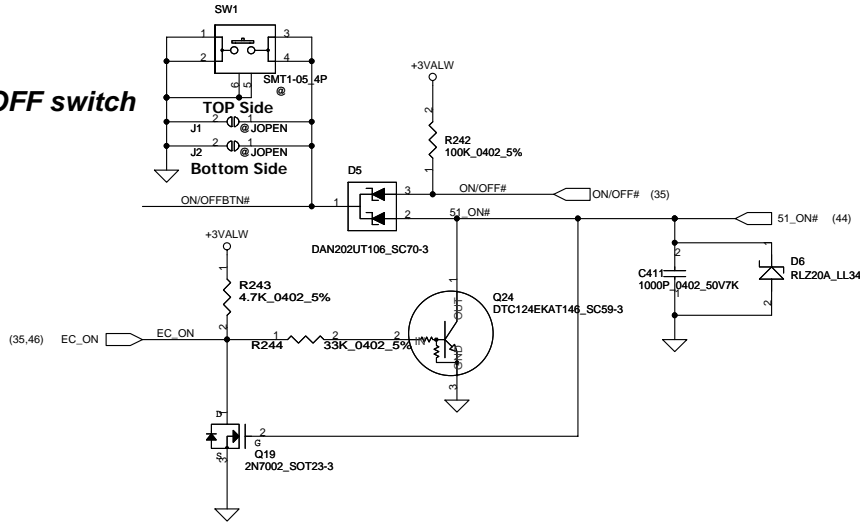
CMOS Camera Conn



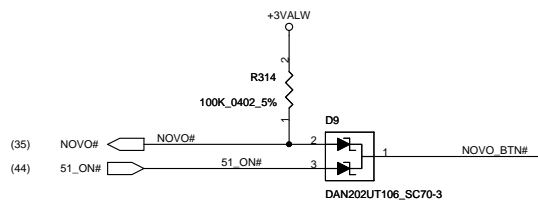
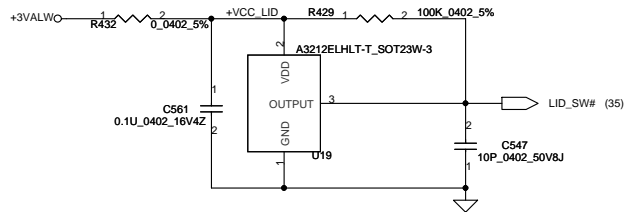
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								Document Number		Rev 1	
								401557			
								Date		Sheet	
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Power Button

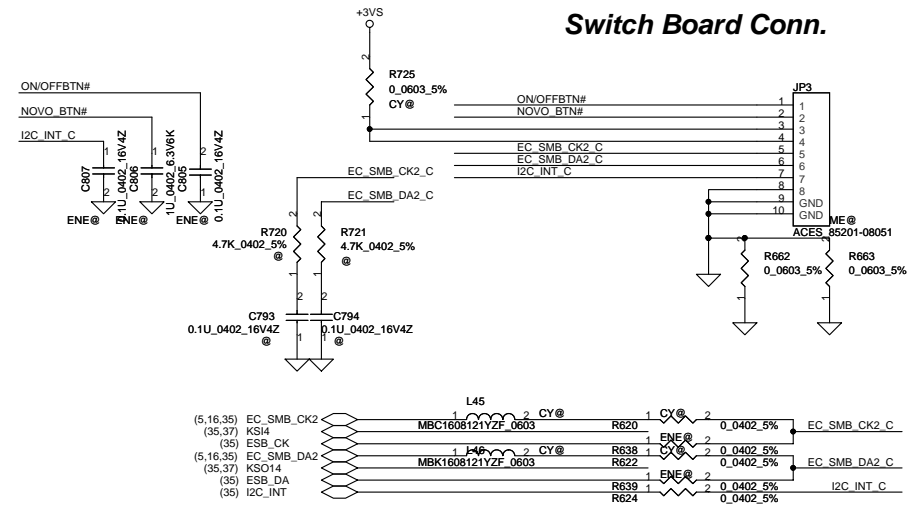
ON/OFF switch



Lid Switch

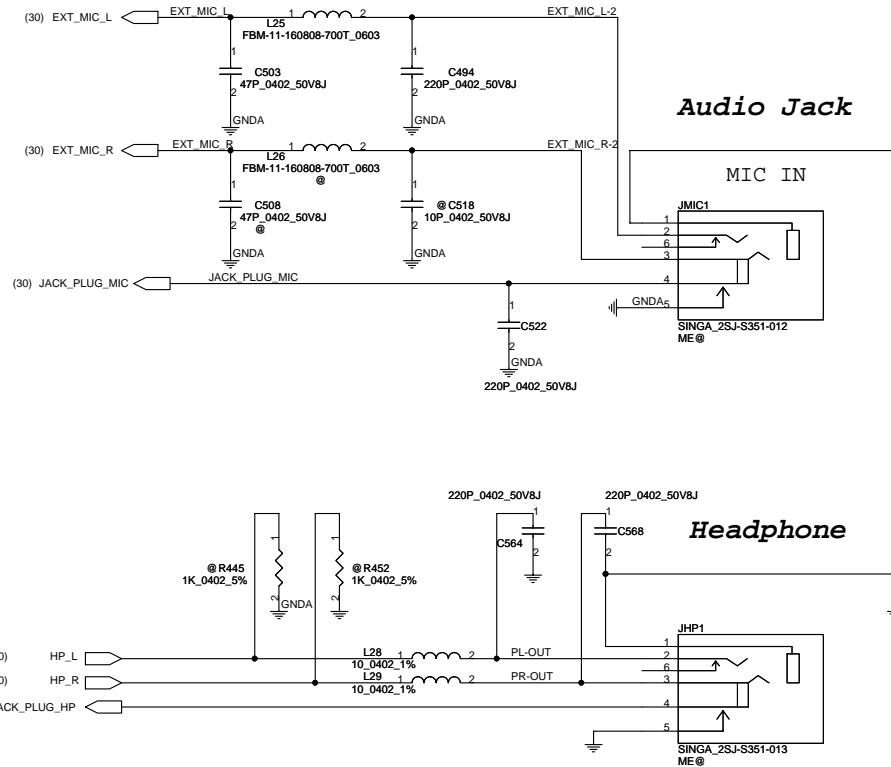


Switch Board Conn.



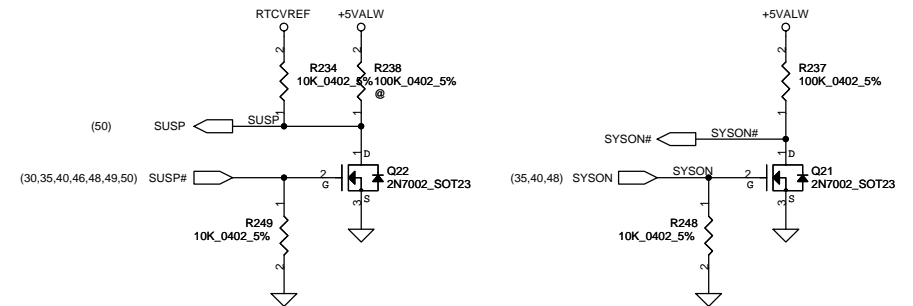
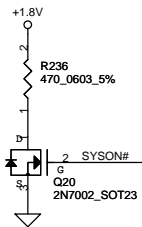
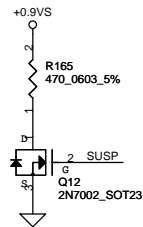
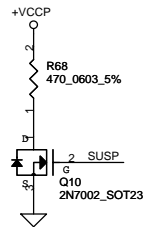
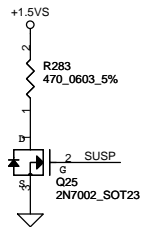
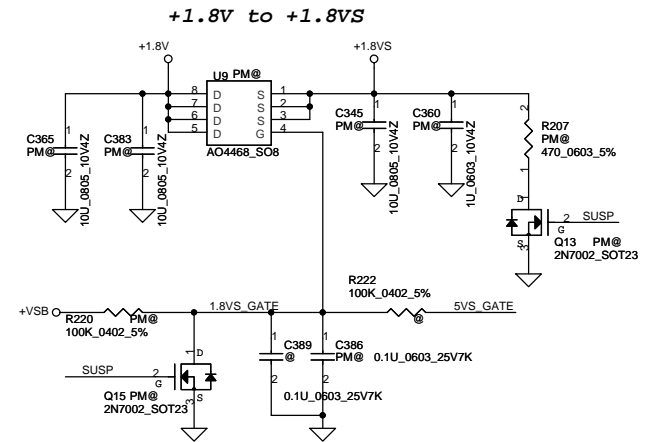
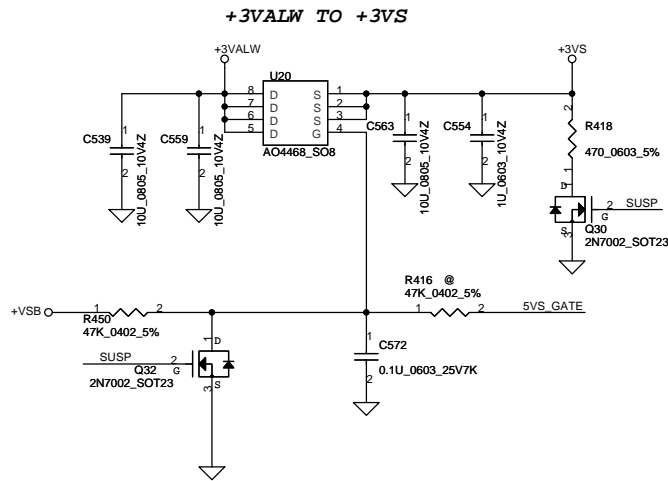
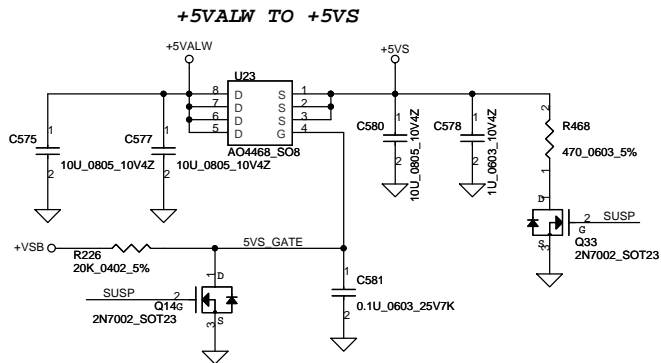
8 mil

Audio Jack

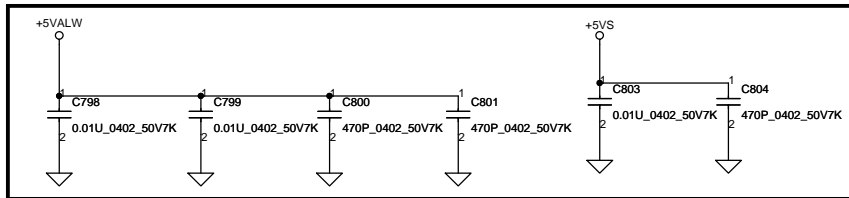


Headphone

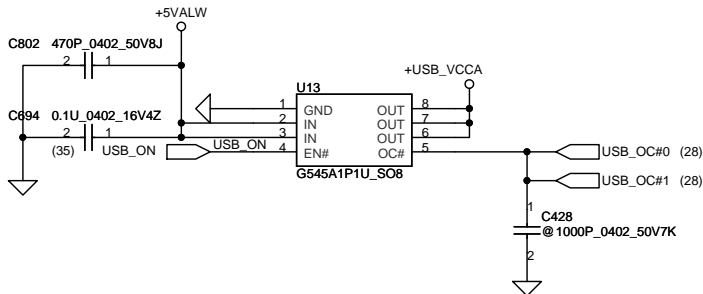
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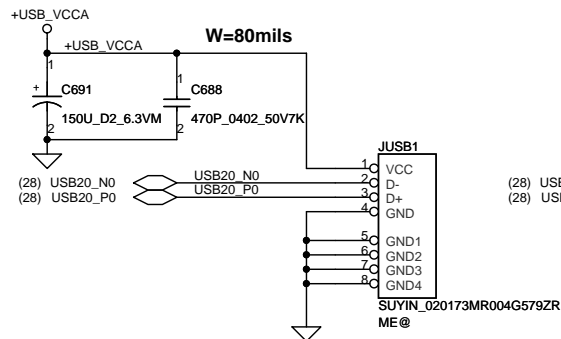
for EMI



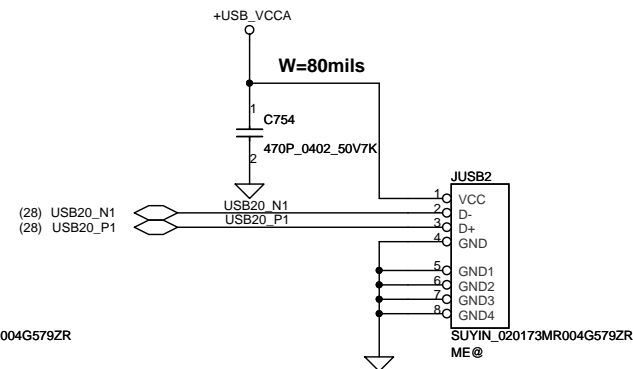
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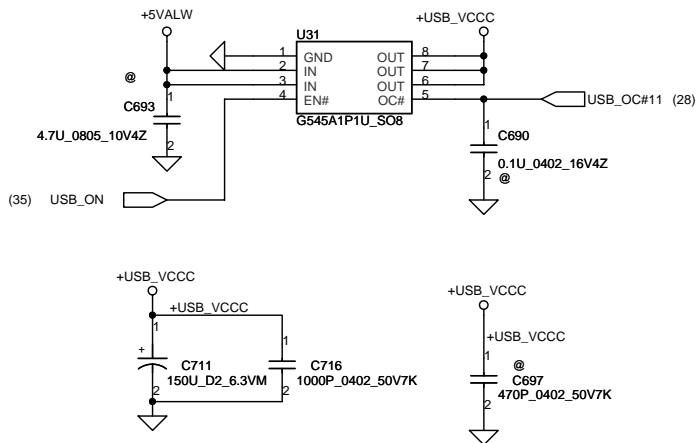
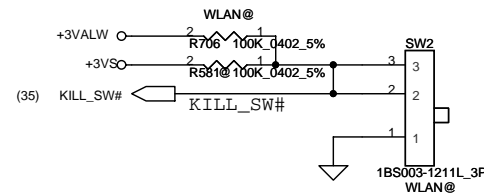
LIFT USB CONN. 1



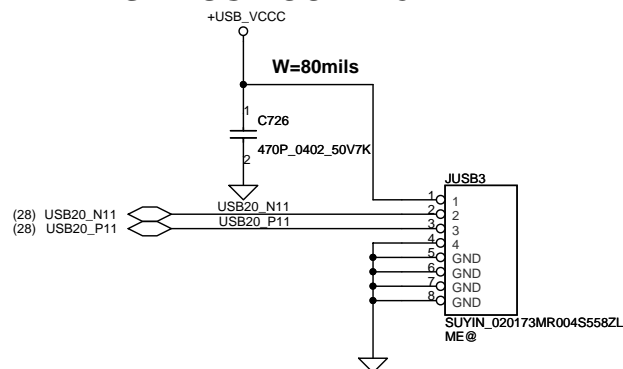
LIFT USB CONN. 2



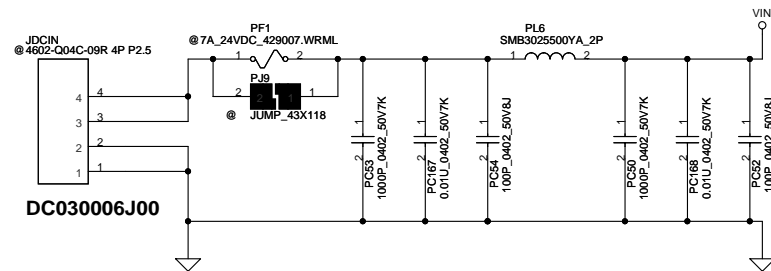
Kill Switch



RIGHT USB CONN. 3



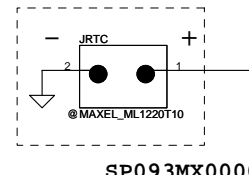
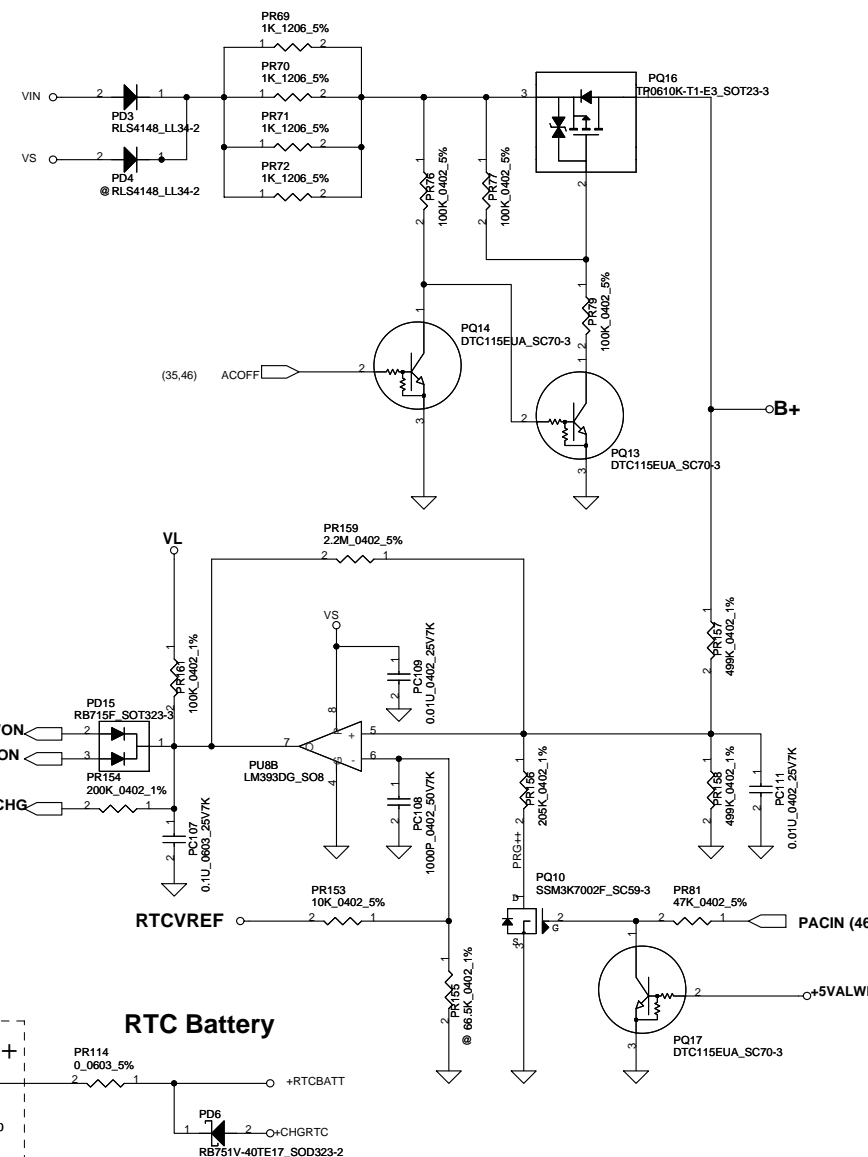
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Vin Detector		
High	18.135	17.01
Low	14.866	14.355

ACIN			
	Precharge detector		
	Min.	typ.	Max
H-->L	13.843V	14.247V	14.636
L-->H	14.936V	15.381V	15.814

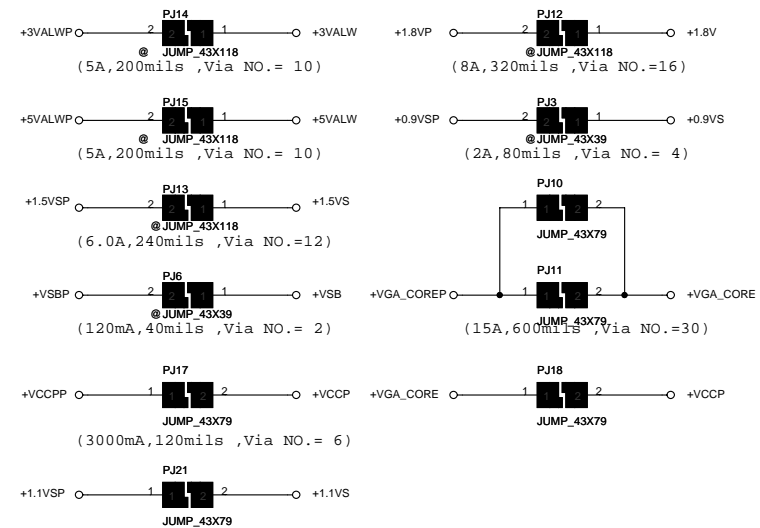
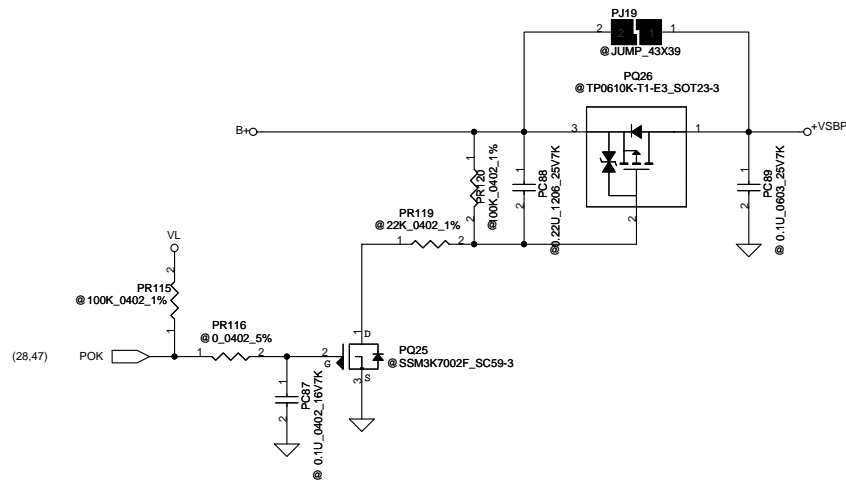
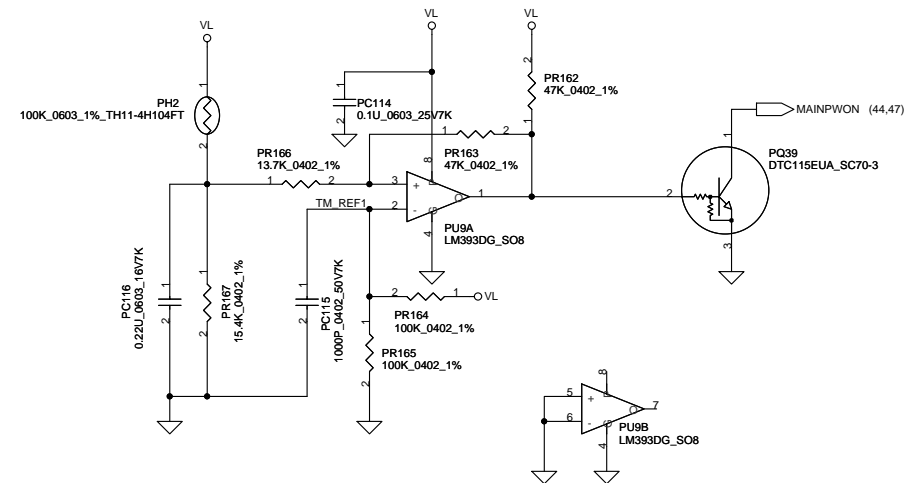
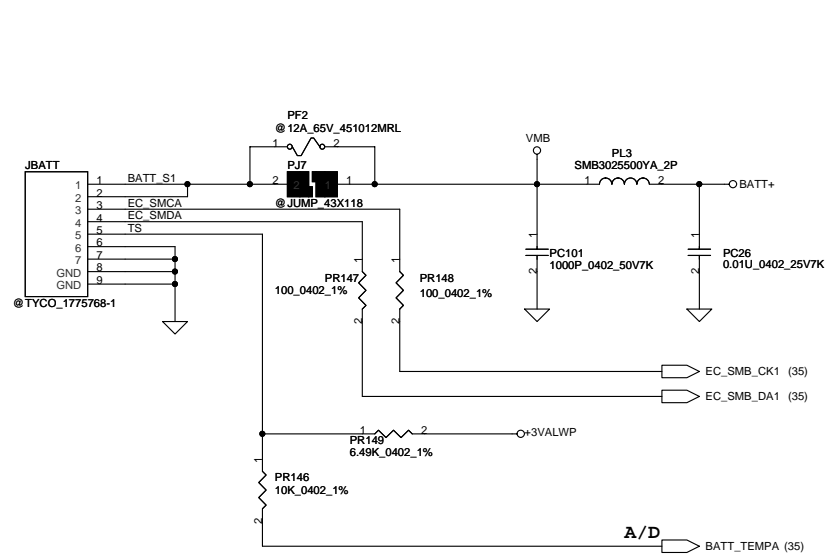
BATT ONLY			
	Precharge detector		
	Min.	typ.	Ma
H-->L	6.138V	6.214V	6.359
L-->H	7.196V	7.349V	7.505



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PH1 under CPU botten side :

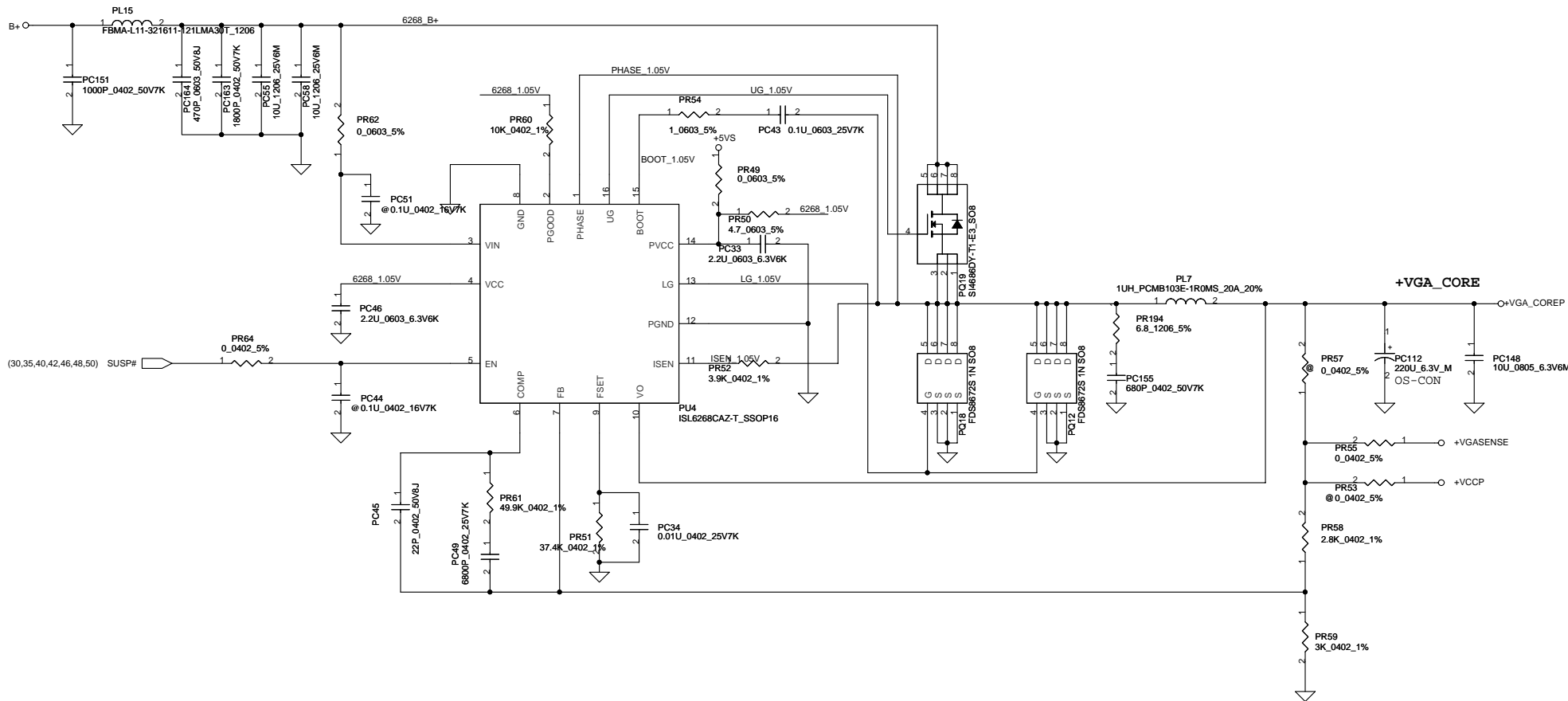
CPU thermal protection at 92 degree C
Recovery at 56 degree C



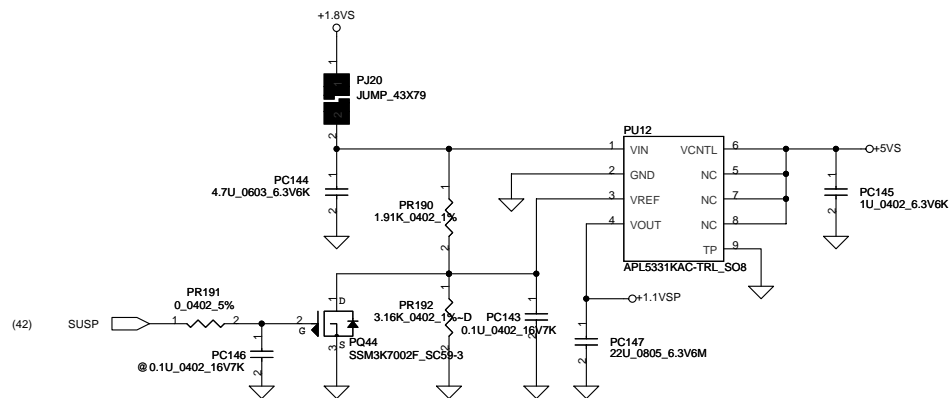
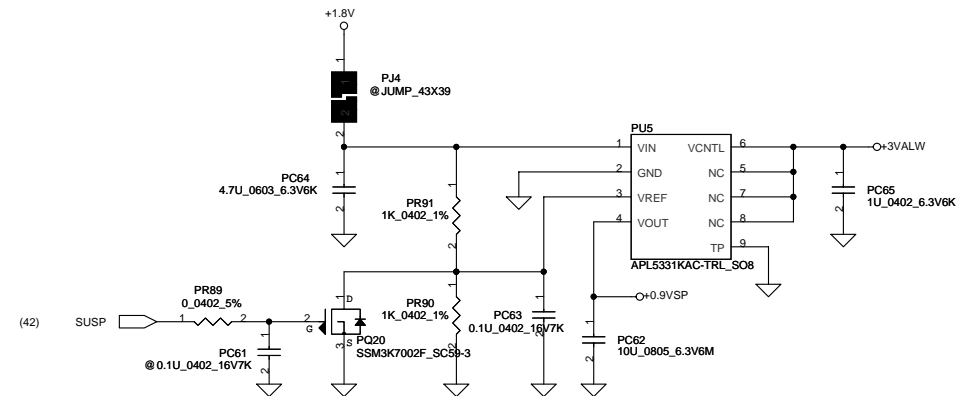
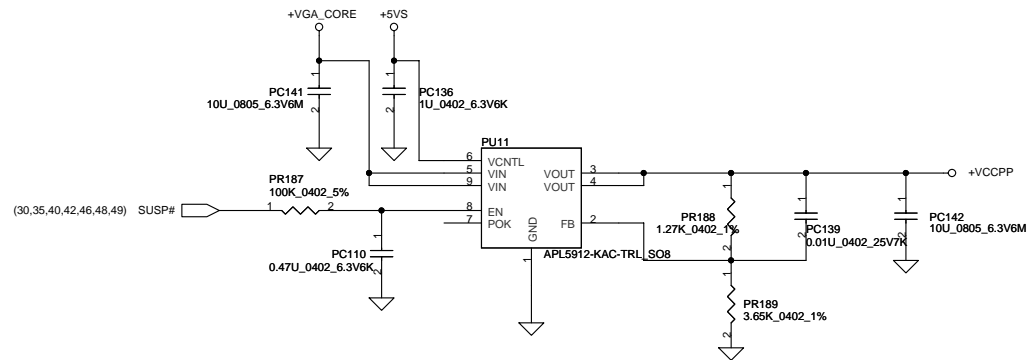
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
10/12		P48	Add PR185, PR186	Reserve for debug use.
10/12		P49	Delete PC110	Because HW reserve enough CAP.
10/17		P49	Add PU11, PC136, PC141, PC142, PC139, PC110, PR187, PR188, PR189	Because need separate +VCCP and +VGA_CORE
10/17		P49	Change PR58 from 2.7k_0402_1% to 2.8k_0402_1% PR59 from 3.24k_0402_1% to 3k_0402_1%.	HW request change VGA_CORE from 1.1V to 1.16V

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